VACUUM FIELD EMISSION MICROELECTRONIC DEVICES BASED ON SILICON NANOWHISKERS

A thesis

submitted in partial the fulfilment

of the requirements for the degree

of

Master of Electrical and Computer Engineering

at the

University of Canterbury

by

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ABSTRACT

Vacuum field emission devices have become a promising candidate for emerging display technology due to their interesting properties compared to conventional thermionic emission devices that require high temperature and power to operate. Unlike thermionic emission, field emission devices can induce the electrons to emit at low temperature; sharp and thin emitters on the cathode are desired in order to increase the field emission. Many candidates from other research groups, such as Carbon Nanotubes (CNTs), SiC and ZnO, appear to have high field emission, but their complicated fabrication processes are the drawback.

The silicon nanowhiskers produced by Geological & Nuclear Sciences (GNS) using Electron-Beam Rapid Thermal Annealing (EB-RTA) are an alternative material that is fast, inexpensive and uncomplicated to produce. They are based on the thermal desorption of silicon oxide, which forms silicon nanowhiskers on the silicon wafer in a short duration.

Field emission diode structures on Silicon on Insulator (SOI) wafers were fabricated in order to investigate the field emission due to these GNS silicon nanowhiskers. An uncomplicated fabrication process using photolithography and etching process was developed. Electron beam lithography (EBL) was also used to create the different feature sizes directly onto the SOI wafer. The silicon nanowhiskers grown on these structures are as high as 35 nm with density distribution up to 30 μm^{-1}. The electrical characteristics of these devices are diode-like when the voltage range from -40 V to 40 V is applied. The best samples produced an emitted current as high as 2 mA, which is suitable for many applications, such as flat panel displays, x-ray sources and high frequency devices. However, in some cases, the diode structures failed to show the diode-like characteristics, perhaps as a result of bad contact connections or the emitters have been worn out after applying high voltage for some time. Device life time and stability were also considered and investigated via a number of electrical measurements for a period of time as long as one hour in this study. Even though these nanowhiskers have shown promising results, there are still many aspects to be considered to improve the experiments, such as the vacuum system and better contacts.

ACKNOWLEDGEMENTS

I would like to express my deep gratitude to my supervisor, Professor Richard Blaikie and my co-supervisor Dr Stuart Lansley, for their guidance, constructive suggestions and encouragement throughout this project. Their brilliant suggestions and useful instructions in semiconductor processing made this project possible. I also would like to thank Dr Steve Johnson, Dr Andrea Markwitz and Dr Mario Rudolphi from Geological & Nuclear Sciences (GNS) for providing the silicon nanowhiskers for this project. Their expertise helped me gain great understanding about nanowhiskers.

I also would like to acknowledge staff in Electrical and Computer Engineering especially Helen Devenreux and Gary Turner, for their kind help in the Microelectronics Laboratory. Thanks are also extended to the members in Nanotechnology Research Group, particularly Leo, Martin, James, Keke, William, Alan, Lin, Andrew, Volker, Dave, Erwin and Patrick for sharing their experimental knowledge and creating a good working environment in the laboratory.

Finally, I am sincerely grateful to my family and friends, Samara, Li Zhou, William, Wallace, Chun Hong, Alan, Seung Ho, Jerawala, Sutida, Mel, Angie, Priscilla and Erwin, for their love and support, without which this thesis would have been more difficult.

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CHAPTER ONE

INTRODUCTION

At the present time, there are many aspects in our personal life that are going to be transformed by nanotechnology. Not only are computers and electronic devices getting smaller, more powerful and cheaper, but biotechnology has also become more advanced as we can manipulate matter at the molecular and atomic level. Nanostructured materials and devices provide links between molecular and solid-state physics and eliminate some of the limitations of conventional technologies. These nanostructures have the potential for applications such as battery electrodes [1], gas sensing [2], supercapacitors [3] and field emission display for flat-panel TVs [4]. Hence researchers are focused on investigating and developing nanostructured materials, particularly silicon nanostructures that can be combined with the power of modern silicon integrated circuits.

Emerging vacuum microelectronics devices are of much interest due to their unique properties such as high current densities, ballistic electron transport, temperature independence and radiation hardness. These properties promote a wide range of applications including field emission displays (FEDs) for flat panel monitors. Many research groups have developed field emission devices based on nanostructured material such as carbon nanotubes (CNTs) [5-9], nanobelts [10-11], SiC nanowires [12-14], AlN nanoneedles [15], Si nanowires [16], SnO_2 nanowhiskers [17] and so forth. Generally, fairly high emission current density, i.e. $10mA/cm^2$, is desirable to light a phosphor display. Electron emission from CNTs, nanowires and nanowhiskers has been mainly attributed to their tips with small radii of curvature; thus, aligned growth should give high-current emission due to increased number of active emitters per unit area.

Currently silicon is probably the most important material in the semiconductor industry, and it is regarded to be one of the main materials in field emission devices. Thin whisker-like structures, called nanowhiskers, that can be grown on a silicon surface are one possible alternative for field emission devices [18]. Silicon

nanowhiskers have been studied by many research groups around the world, including a group at Geological & Nuclear Sciences (GNS) in New Zealand. The research described in this thesis is the result of a collaboration with GNS to investigate silicon nanowhiskers and their potential use as field emission devices.

This chapter provides the outline of this thesis. It lays out the background of nanowhiskers, vacuum microelectronics and potential applications that has motivated this research. It also describes the field emission device fabrication and other whisker-like structures for field emission devices that have been studied by other research groups. Finally, the arrangement of this thesis is presented.

1.1 Motivation

GNS has developed the silicon nanowhisker fabrication process using electron-beam annealing (EBA) [19]. They have successfully fabricated silicon nanowhiskers using untreated silicon substrates. Although many nanostructured materials have been used to fabricate field emission devices, a motivation to investigate the capability of silicon nanowhiskers as field emitters in vacuum microelectronic devices is enormous due to their promising properties. The challenge now is to grow silicon nanowhiskers using various types of wafer, such as Silicon on Insulator (SOI) and investigate their formation mechanisms, electrical characteristics, lifetime, stability and potential applications. This research also aims to optimise the nanowhisker growth conditions and test the properties of field emission in order to produce a vacuum microelectronics device that is uncomplicated and inexpensive to produce.

1.2 Overview of Vacuum Electronics

The practice of using controlled electron propagation in a vacuum to obtain signal gain has been around since American inventor Lee De Forest introduced the triode vacuum tube in 1907 [20]. Vacuum electronics use the mechanism of electron emission into a vacuum. By fabricating arrays of conductive or semiconductive structures that are either gated or ungated, the devices can be formed by utilising cold emission and ballistic transport of electrons from emitting cathodes to appropriate

collector electrodes. Integrated solid-state devices have taken over as cheap, versatile and robust alternatives to vacuum electronics. However, there are certain applications where solid-state devices are impractical, and a potential solution is the same vacuum technology that has been forgotten for nearly 50 years. Potential applications include flat panel vacuum displays [21], ultrahigh-frequency power sources and amplifiers, e.g. microwave tube power amplifiers, electron and ion guns and x-ray sources, high-speed logic and signal processing circuits, miniature electron-beam lithography systems, electron microscopes and microprobes, and sensors [22]. A number of vacuum microelectronics devices have moved beyond the research laboratories to actual prototypes and commercial products, such as PixTech, Canon and Toshiba, Nano-proprietary, Inc., Motorola and Futaba [23-28].

In some applications, solid-state devices are not suitable due to their sensitivity to harsh environments. For instance, the sensing electronics in space are subjected to high levels of radiation. This radiation can produce charge carriers in the bulk solid-state devices which can cause transient artifacts in the operation of the device and some permanent damage. An obvious solution to this problem is to use a radiation protecting material, such as carbon. Other options are to use radiation-hard fabrication techniques and silicon-on-insulator (SOI) substrates, which have been claimed to reduce radiation-induced problems. However, these solutions require very inefficient circuit design to achieve maximum radiation damage protection. Unlike solid-state devices, vacuum electronics use a vacuum channel in which it is not possible to induce carrier generation through radiation. Thus, vacuum electronics are suitable for the high radiation environment as devices are relatively immune to radiation damage. Another application that vacuum electronics are potential good for is aircraft and machine sensing applications that require high temperature operation. In both applications, the sensors have to be placed on high temperature surfaces to sense various functionalities [22]. A current solution to this problem is to place electronics away from the sensor. This introduces efficiency and accuracy problems as long wires between the sensor and electronics are required. Similar to vacuum devices' inherent immunity to radiation, their vacuum channel does not generate thermally induced carriers. In other words, they are inherently tolerant to high temperatures; therefore vacuum electronics are still popular in the high-power RF transmission community.

Vacuum electronics can be separated into two categories: thermionic emission or field emission. The difference between these two categories is the way electrons are emitted from the cathode. In both cases, the emitted electrons are accelerated towards the anode through a vacuum channel.

1.2.1 Thermionic Emission

Thermionic emission relies on a cathode which is a heated electron emitter. The cathode is heated up until the electrons receive enough kinetic energy to leave the surface of the cathode. Thermionic devices have the obvious disadvantage that every device needs a heating element. Thus, the material used in these devices must be able to tolerate a temperature of at least 1000K to induce electron emission.

1.2.2 Field Emission

Unlike thermionic emission, field emission is possible with a cold cathode. Although field emission has the obvious advantage of not requiring a heating element, the fabrication of these devices presents multiple problems. The field emission highly depends on the size and work function of the emitter. A cold cathode becomes more power efficient as smaller emitter sizes are achievable using modern IC fabrication processes. Therefore, field emission is the preferred integrated solution. Field emission occurs when an electric field above approximately 0.5V/Å is placed on a metal surface in a vacuum [29]. It is necessary to use a needle-sharped emitter to achieve uniform emission with an acceptable anode voltage. Usually the field electron emission easily occurs at sharp tip known as emission site. The electric field at the emission site is normally enhanced over the averaged electric field by a factor according to the geometrical structure of the emission site. This factor is almost inversely proportional to the curvature radius of the tip of the emission site [30]. Hence, by reducing the emitter radius, we can increase field enhancement, allowing a lower anode voltage, so this device is more useful. Therefore, researchers have emphasised the need for reliable and reproducible fabrication of sharp emitter structures. One of the promising sharp emitters with low work function and high field enhancement factor is silicon nanowhiskers developed by GNS.

The concept of field emission arrays (FEAs) was introduced in early 1960s to enhance the emission current [31]. In the semiconductor industry, Si is one of the most common materials and unsurprisingly, silicon-based micro-fabrication ungated FEAs were demonstrated some time ago [32]. Many research groups have developed innovative nanostructure fabrication techniques to improve the aspect ratio and hence the field emission. Silicon nanostructure fabrication techniques using electron beam lithography for the high resolution structures provides high uniformity and precise dimensional control. However, the low throughput associated with electron beam lithography is a disadvantage that prevents it from being used as an industrial nanofabrication tool. A bottom-up approach is an efficient alternative which involves manipulating individual molecules and builds the nanostructures from these. These molecules can be manipulated by many techniques such as DNA self-assembly [33], quantum dot self-assembly [34] and electron-beam rapid thermal annealing (EB-RTA) [18-19].

Nanostructured silicon (100) forming EB-RTA developed by GNS is one of the most promising techniques for silicon nanostructures. This process is exceptionally rapid and uncomplicated; with growing occurring at 1100 ºC for 3s of annealing without any pre-treatment or cleaning of the Si surface [19]. Field emission characteristics of these self-assembled silicon nanostructures are stable, have lower power consumption and are reproducible with emission occurring at very low threshold fields. Therefore, the possibility of using Si self-assembly for fabricating as a field emission cathode is promising. The mechanism and formation of the nanowhiskers will be discussed in Chapter 2.

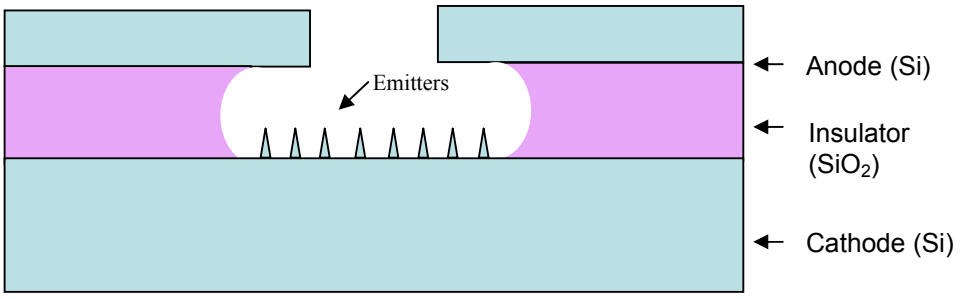


Figure 1-1 Schematic cross section of field emission device using SOI wafer.

Figure 1-1 shows the cross section of a typical vacuum field-emission device having nanostructures grown on the cathode surface as the emitters. In this research, silicon-on-insulator (SOI) was used because of its simplicity in fabrication; detailed explanation will be provided in the next chapter. For this type of emission, the extraction force comes from an electric field. When the cathode is put at a different potential to the anode, the electric field from the conductor will exert force on the free electrons in the semiconductor. If the positive field is high enough, the free electrons will succeed in overcoming the restraining force of the surface and emission will occur. Normally the electric charge is not distributed uniformly unless the conductor is in the shape of a sphere. Rather, charge concentrates at places of greatest curvature. Hence, the smaller the radius of the conductor, the more charge will be found at the tip, and the higher electric field will be.

A negatively charged cathode is used in a field emission device. This type of display uses an applied voltage to create an enhanced electric field at the tip that electrons can engage in a phenomenon known as tunnelling as escape into free space without need for heating the cathode to release electrons. Normally, in order to escape the conductor, electrons must have enough thermal energy to overcome that potential energy barrier. By supplying an external electric field, the conductor changes the shape of the potential energy barrier charges, becoming thinner and thinner as the electric field increases. Eventually, the electrons can go all the way through the barrier.

In general, the current-voltage characteristics of field-emission between the cathode tip and anode was confirmed, expressed by the Fowler-Nordheim equation [35];

$$I \propto E^2 \exp\left(\frac{-B\varphi^{3/2}}{E}\right) \tag{1.1}$$

where B is a constant, E is the applied electric field and φ is the work function, the minimum energy required for an electron to be liberated it from the surface of a particular material in eV.

1.3 The Variety of Silicon Whisker-like Structures

As mentioned earlier, many materials have been used as field emission cathodes including CNTs, SiC, ZnO and silicon. Silicon has advantages of being compatible with the existing CMOS technology and being inexpensive, thus it has been investigated intensively for the past decades. A variety of silicon whisker-like structures have been reported using different techniques such as vapour-liquid-solid (VLS) growth and laser fabrication. The bottom-up approach, particularly VLS growth, is one of the most interesting techniques because it can produce small features with size down to 100nm [36-38]. Chemical vapour deposition (CVD) and molecular-beam epitaxy (MBE) are two typical bottom-up approaches for nanostructure fabrication that can provide smaller features. However with their defined radius, length, and position, they turned out to have limited applications in the past. In 2004 Schubert and co-workers reported silicon nanowhiskers in a diameter range of 70-200 nm on <111>-oriented silicon substrates by molecular-beam epitaxy [39]. This VLS growth process was initiated by using small clusters of gold at the silicon interface as seeds, as shown in Fig. 1-2.

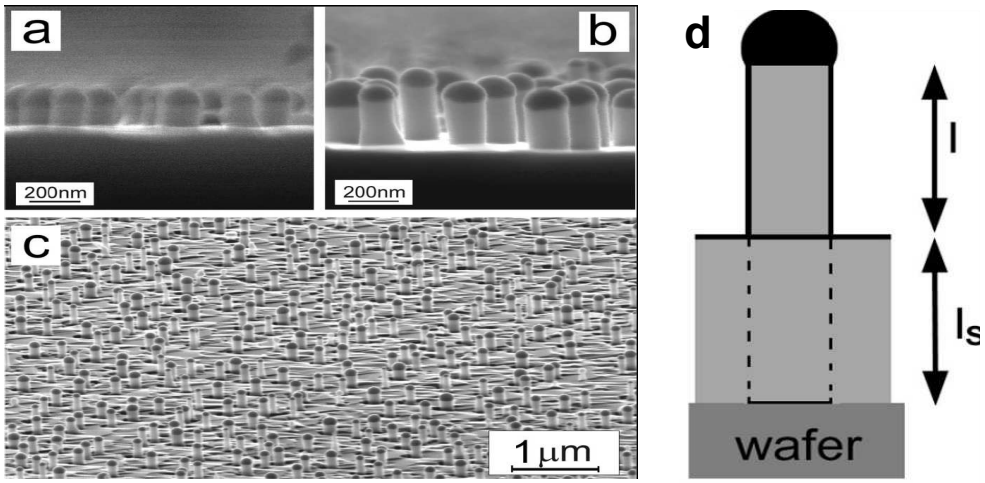


Figure 1-2 SEM images of Si whiskers grown on a <111> Si substrate at 0.5 Å/s for (a) 60 min (b)120 min at temperature T_s = 525 °C. The sample (b) was tilted to get an overview on the arrangement of the whiskers (c). A schematic of Si whisker structures are shown in (d) [39].

The Si nanowhiskers grown by MBE have promising aspects including small feature sizes, but the growth rate and uniformity of distribution needs further consideration for field emission device manufacturing. Schubert *et al.* produced Si nanowhiskers at low temperature of 525 °C for 60-129 minutes. Si nanowhiskers grown by GNS using electron beam annealing take only 3s [18]. In comparison, Si nanowhiskers grown by GNS have advantage over that grown by MBE technique in term of growth rate.

1.4 Potential Applications

The whisker-like structures can be applied in many applications, including optoelectronics, sensors, x-ray sources and cathodes in vacuum microelectronics. Most of those applications utilise their high aspect ratios that provide high field emission with low voltage operation power consumption. Similar to conventional thermionic vacuum microelectronic devices, field emission devices can be used as active elements in circuits, particularly in integrated circuits, due to their small sizes. The ballistic electron transport in vacuum microelectronics devices provides short transit times compared to solid state devices. Thus field emission devices are able to operate at higher frequencies with adequate efficiencies. However, at low frequencies, field emission devices create fluctuation noise for high current which may not be suitable in some applications.

The typical application described here is a field emission display (FED), which has been a prospective flat screen technology for over 20 years but reliability and longevity issues have prevented it from leaving the laboratory. Unlike the thermionic cathode in conventional a Cathode Ray Tube (CRT), the field emission cathode can operate at low temperatures, hence no warming up time and high power are required. FEDs not only conserve the image quality and viewing angles of CRT, but they also provide high brightness, reduced display depth, and lower power consumption, making them suitable for larger flat screens. Samsung demonstrated a working CNT display prototype of field-emission display with 30 inch diagonal screen in 1999 [21]. Silicon nanowhiskers have similar properties as CNTs; they certainly are alternative field emitters which can be easily produced by EBA in a very short time.

Other applications such as x-ray sources, microwave tubes and electron guns also utilise the small feature sizes of the nanowhiskers which can promote high field emission current at low temperature. Furthermore, some atomic scale measuring equipment such as Scanning Tunneling Microscopes (STM) and Atomic Force Microscopes (AFM) can be made from those whisker-like structures due to their extremely small sizes [40]. The application of field emitter arrays to ion source technology has been reasonably wide spread, including electron impact sources, field ion emission sources and liquid-metal ion sources. The main advantage of these applications is that electron beams can be produced by a voltage lower than 100 V with a power consumption of only a few miliwatts [41]. Many more applications have been presented in the past decades and surely the number of applications will continue to grow as we begin to gain more control of fabrication conditions and techniques.

1.5 Thesis Arrangements

The remainder of this thesis is organised as follows. Chapter Two describes the background of silicon-on-insulator (SOI) wafer, silicon oxidation, void formation and its kinetic mechanisms of those nanostructures growth using the GNS fabrication technique. The temperature and time dependence of these nanostructure characteristics will also be discussed in detail. Furthermore, the density and duration dependence of the Si nanowhiskers will also be described.

Chapter Three presents the fabrication techniques and processes used to produce these field emission devices. The description of the equipment used in this research will also be presented. The main processes involved in fabrication of the diode structures are diffusion, photolithography and etching. The imaging techniques, such as AFM and SEM used to analyse the sample surface will also be discussed.

Chapter Four covers the experimental results, including the diode structure produced by the fabrication techniques described in Chapter Three, and the surface characteristics of the sample before and after annealing, showing the promising results in terms of height and density distribution. Electrical characteristics of the diode

structured devices produced by different conditions are presented. For field emission devices, the field emission or emitted current characteristics are also discussed as they have significant effects on their performance. In addition, life and stability of the field emission devices will be considered. Finally, the results of light emission from a phosphor screen will be presented.

Chapter Five discusses the fabrication issues that may effect the diode structure fabrication, electrical measurements and surface imaging techniques. This chapter also presents the application of silicon nanowhiskers and some possible experimental improvements. Finally, conclusions and discussion of possible future work are presented in Chapter Six.

CHAPTER TWO

BACKGROUND

This chapter will give a background of SOI wafer technology, silicon oxidation which explains how silicon oxidation and void formation occurs, and the growth of nanowhiskers via oxide desorption and oxidation kinetics. The Separation by Implanted Oxygen (SIMOX) wafer was used to create microelectronic devices, such as field emission diodes. Field emitters are required for this field emission device; therefore, it is important to understand the nanowhisker growth mechanism and dependent conditions.

2.1 Silicon on Insulator (SOI) wafer

SOI was first investigated in Japan in 1978, when Nippon Telegraph and Telephone (NTT) developed the SIMOX process and gave the first demonstration of an SOI device [42]. SIMOX was essentially the only available SOI wafer technology until early the 1980s, when wafer-bonding technology was invented [43]. Then Mitsubishi produced a low-power gate array in SOI in 1997 [44]. After that fully depleted SOI-based system-on-chip (SoC) LSI chips which have been integrated into Casio watches were developed by Oki Electric [45]. The insulation (SiO_2) in SOI wafers reduces the leakage current, which allows designers to create devices that are faster and consume less power (up to 80% loss) than traditional bulk silicon.

SIMOX SOI and wafer bonding SOI are the most prominent technologies used in the market. SIMOX SOI wafer fabrication process starts with the bulk silicon substrate and then oxygen ions are implanted into a polished wafer. The wafer is annealed at high temperature to form a buried oxide (BOX) layer at a uniform depth from the surface and to eliminate the defects made in the surface layer, as shown in Figure 2-1.

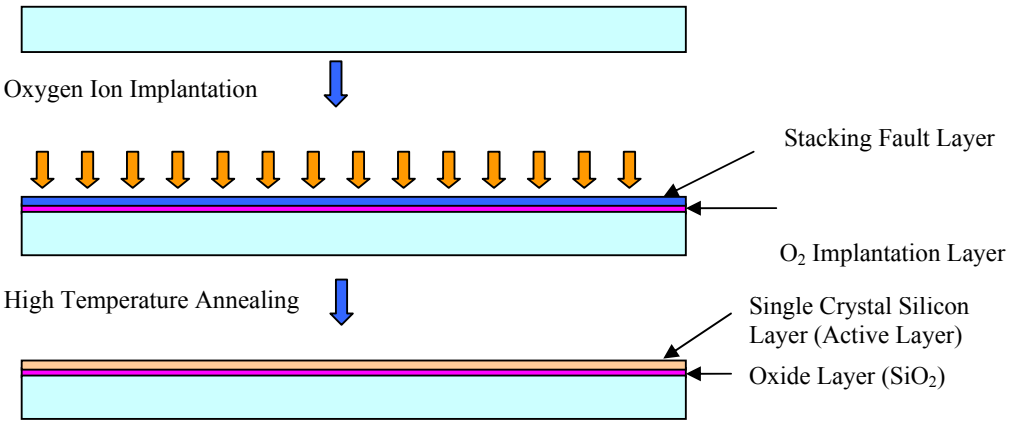


Figure 2-1 Fabrication of SIMOX SOI wafer

SIMOX involves the direct injection of purified oxygen into the silicon wafer at an extremely high temperature. Then the oxygen bonds with the silicon and forms a thin layer of silicon oxide. The thickness of the silicon oxide layer can be changed by an increased oxygen implantation dose. This layer of silicon oxide film is then bonded with the pure crystal silicon layer [46]. The SIMOX wafer that has been used in this study has a 280nm thick silicon layer on top of a 380nm thick of SiO_2 layer separating the Si substrate and the top Si layer. One of the important issues that is addressed here is the formation of Si nanowhiskers on SOI wafers, as previous studies at GNS have concentrated on single-crystal silicon only.

2.2 Silicon Oxidation

Silicon dioxide (SiO_2) is one of the most important ingredients in semiconductor industry, playing a crucial role in the development of semiconductor planar processing. Silicon dioxide is a high quality electrical insulator that can be used as a barrier material in impurity implants or diffusion, or for electrical isolation of semiconductor devices. The reverse reaction called oxide desorption is also crucial in microelectronics technology.

2.2.1 Formation of Silicon Oxide

The formation of SiO_2 on a silicon surface is often achieved through a process called thermal oxidation. Thermal oxidation is a technique that uses high temperatures, normally between 700-1300 °C, to promote the growth of oxide layers [19]. The thermal oxidation of silicon involves exposing the silicon substrate to an oxidation environment of oxygen (O_2) or water vapour (H_2O) at extremely high temperature, producing oxide film which thicknesses range from 60 to 10000 Å [47]. Oxidation of silicon is not difficult to achieve, since silicon has a natural reaction to vapour or oxidising ambient at room temperature forming thin oxide layer, know as "native oxide". However once the oxide layer is formed, the oxygen atoms have to diffuse through oxide layer to react with the silicon interface. Hence the thickness of native oxide layer will not exceed 25 Å, because the mobilities of either silicon atoms or oxygen molecules are not sufficient in room temperature conditions. The elevated temperature used in thermal oxidation therefore accelerates the oxidation process resulting thicker oxide layers per unit time.

Thermal oxidation can be accomplished by either using "dry oxidation" (wherein the oxidant is O_2) or "wet oxidation" (wherein the oxidant is H_2O) depending on the oxidising agent used. The reactions for dry and wet oxidation are described by the following equations [47]:

dry oxidation: $Si(solid) + O_2(gas) \rightarrow SiO_2(solid)$ and

wet oxidation: $Si(solid) + 2H_2O(vapour) \rightarrow SiO_2(solid) + 2H_2(vapour)$. (2.1)

During dry oxidation, the mobilities of silicon and oxygen atoms are highly dependent on the ambient O_2 concentrations, pressure and temperatures. Thus the thickness of the oxide can be increased by increasing O_2 concentration and pressure with appropriate temperatures. In wet oxidation, hydrogen and oxygen gases are introduced into a chamber where they react to form water molecules, which are made to diffuse toward the silicon surface. The water molecules react with the silicon atoms to produce the silicon dioxide and another byproduct, hydrogen gas.

The oxidation reactions occur at the Si-SiO_2 interface resulting in consumption of silicon at the interface as oxidation takes place. The Si-SiO_2 interface moves into the silicon substrate as the oxide grows, as a result, the Si-SiO_2 interface will always be below the original Si wafer surface, whilst the SiO_2 surface is always above the original Si surface. The rate of oxidation formation during oxidation processes that have very long durations may be modeled by the *Parabolic Growth Law* [48]:

$$x_0^2 = Bt, \tag{2.2}$$

Where x_0 is the thickness of the growing oxide, B is the parabolic rate constant, and t is the oxidation time. This shows that the oxide thickness growth rate is reduced as the oxide thickness increases because the oxidizing species have to travel a longer distance to the Si-SiO_2 interface.

On the other hand, the oxidation process that has very short durations may be modeled by another simple equation know as the *Linear Growth Law*:

$$x_0 = C(t + \Gamma), \tag{2.3}$$

where x_0 is the thickness of the growing oxide, C is the linear rate constant, t is the oxidation time and Γ is the initial time displacement. However, a far more accurate model of oxidation process over a wide range of temperatures (700-1300 °C), oxide thickness (300-20000 Å) and oxidant partial pressures (0.2-25 atmospheres) is called *Linear Parabolic Model* (or Deal-Grove Model), developed by Deal and Grove [47].

The opposite reaction of thermal oxidation is thermal decomposition which occurs when low O_2 partial pressure is applied with high temperatures. The two reactions that occur simultaneously are expressed as follow [47]:

$$\begin{aligned} &2Si(solid) + O_2(gas) \rightarrow 2SiO(gas), \\ &Si(solid) + SiO_2(solid) \rightarrow 2SiO(gas) \end{aligned} \tag{2.4}$$

The first reaction occurs when the silicon surface is exposed to oxygen and reacts with oxygen molecules. As a result, SiO gas is produced, since they are in a low O_2 partial pressure environment. This reaction causes the etching of the Si surface by O_2 with SiO desorption, generating nanoscale holes on top of the sample surface. At the Si-SiO_2 interface, consumption of SiO_2 occurs due to the reaction of SiO_2 with Si as shown in second reaction above. This promotes an increase in the size of the holes and the formation of new holes.

2.2.2 Formation of Voids

The formation of voids is a very important mechanism used to explain how nanoscale islands, know as nanowhiskers, are formed. Some studies have reported that decomposition of an oxide layer occurs locally, that is, nanoscale holes called "voids" grow laterally and increasingly expose clean Si surfaces as the annealing time and temperature increase [18], [19] as shown in Figure 2-2. The growth kinetic of voids in oxide layers has been studied by scanning electron microscopy (SEM) and atomic force microscopy (AFM). Watanabe and his associates discussed mechanism of void growth, as well as change in surface morphology after the decomposition, and their dependence on the oxide layer thickness [48]. They explained that the void density increased as the annealing time and temperature increased, and that as these voids grew they coalesced.

The voids can be generated in a silicon oxide film via reaction between silicon and oxygen. Void formation on thin oxide films and ultrathin oxide films formed at room temperature with oxygen absorption as mentioned previously. At high temperatures and low O_2 pressures, voids are formed via the reaction between silicon oxide films and silicon molecules. The mechanism schematic of void formation in silicon oxide is illustrated in Figure 2-2.

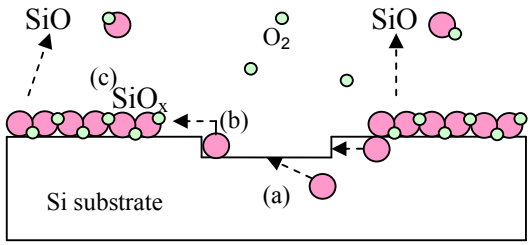


Figure 2-2 Mechanism schematic of void formation in silicon oxide [48].

When a void is created, enlargement occurs via a three-step mechanism as shown in Figure 2-2: (a) Si monomers created from atomic-height holes within the exposed Si surface supply the decomposition and (b) mobile Si monomers migrate to the edge of the void surface where (c) they react with oxygen to form volatile SiO [48]. Previous study has shown that the oxide layer randomly decomposes by forming a volatile SiO phase [49]. Even for a one-molecule thick oxide film, the nucleation sites are independent of the interfacial atomic steps. It has been found that the void density depends on the oxide layer thickness even though we cannot identify the original void nucleation site. These two results indicate that the interfacial structure alone does not determine the void nucleation site.

During annealing voids initiated at defect sites on the silicon oxide surface grow laterally and coalesce. Although nucleation occurs independently of the interfacial steps, the void density increases as the annealing time and temperature are elevated or when the oxide layer becomes thinner. In conclusion, void growth kinetics are governed by the surface mass transport on the exposed Si surface. This void formation and growth kinetics are a significant part of silicon nanowhiskers growth that has been used in this study.

2.3 Growth and formation of silicon nanowhiskers

The formation of nanowhiskers is not an obvious mechanism. A nanostructure growth mechanism has been proposed based on kinetic amplification of the surface disorder as a consequence of decomposition of a surface oxide layer. As mentioned previously, nanostructure growth is initiated by thermal decomposition of the native oxide layer which is known to decompose in high temperature and low oxygen partial pressure environments. This decomposition occurs when the voids form in the oxide film and enlarge laterally across the surface, coalesce and finally spread over the whole sample surface.

This mechanism results in consumption of silicon from the void regions and causes atomic scale surface disorder. The number and size of islands depend on the adatom sea, the mobile atom adsorbed on a surface that migrates over a surface, between islands or the small islands in the surrounding area. The smaller islands often are feed stock for the larger islands during the annealing process. Hence longer annealing times create a lower density distribution of bigger islands.

In this research, the growth of silicon nanowhiskers can be described by two mechanisms. The first process is the oxidation desorption from the native SiO_2 film as already described. The second process is nanocrystal growth regulated by the kinetic of adatom formation, adatom diffusion and adatom-to-island attachment and detachment.

2.3.1 Oxidation Desorption

Nanowhiskers or nanostructures are created via the mechanism of desorption of native oxide layer in low O_2 partial pressure environment. As described in Section 2.2, the void formation can be explained by a three-step process consisting of mobile Si monomer formation, Si monomer migration to the void edges and desorption of SiO. Figure 2-3 figure illustrates how this step-by-step void growth mechanism can also give rise to nanowhisker growth under the right conditions. This requires the kinetics of adatom migration up or down atomic terraces to be such that the growth of small surface irregularities into larger whiskers is encountered.

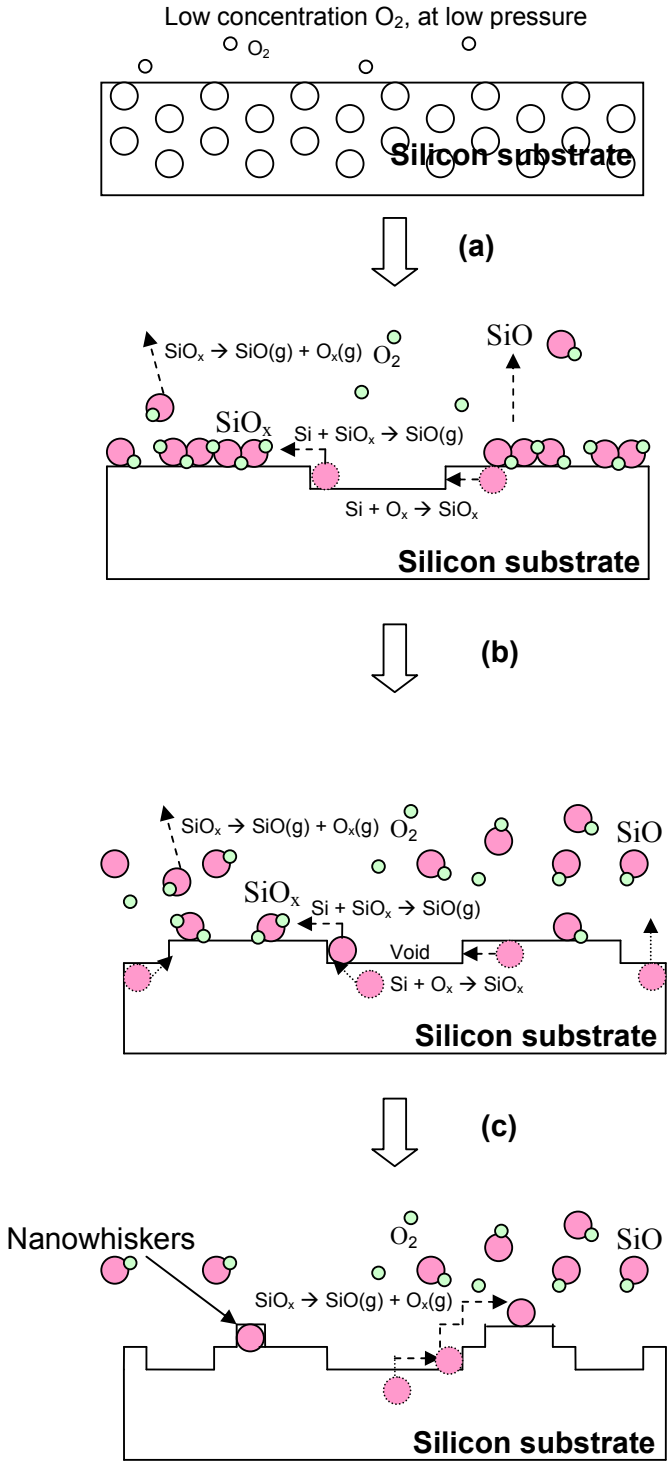


Figure 2-3 Silicon nanowhisker formation via thermal decomposition [48].

The activation energy for diffusion of Si monomers over an ideal Si (100) surface has been reported to be <1 eV, both along and across the dimer rows [50]. During annealing, the diffusive Si atoms created both thermally and by the electron stimulated desorption process, migrate across the void surface in response to the strained potential energy surface resulting from surface disorder. When the potential energy for adatom diffusion at the edge of the step is more than the additional barrier for an adatom to diffuse down the surface step called Schwoebel-Ehrlich barrier [51-52], this promotes bunching of the step once the flow of step is pinned at the given site. The Schwoebel-Ehrlich barrier is a time dependent factor and can be determined by a simple and effective approach [53]. A pit in a step acts as a pinning site creating the growth of the islands around the pinning site.

GNS reported that the activation energy required to activate the Si atoms to move to the upper step and promote nanowhiskers growth is approximately 0.7 eV [18]. The activation energy is increased to 1.1 eV for Si adatoms to move downwards across a step. This activation energy can be altered by changing the annealing temperature. When the temperature is elevated, the mobility of Si adatoms is increased. Thus, higher temperatures tend to promote larger island but lower density. The second mechanism of nanowhiskers growth occurs during cooling down process which will be discussed in the next section.

2.3.2 Nanocrystal Growth

The second stage of the nanostructure growth mechanism, namely nanocrystal growth, is governed by the kinetics of adatom formation, adatom diffusion, and adatom-to-island attachment and detachment. During the process of oxide desorption, the migration of Si monomers generate random numbers of islands with random sizes on the Si surface. The sizes and numbers of islands grow as further adatoms are combined into the islands, supplied either from the adatom sea between the islands or from the smaller islands. The small islands tend to attach to the bigger islands and also know as Ostwald ripening [54]. This attachment and detachment action of the Si adatoms normally occurs during the ramp-down stage of the annealing process. While the temperature is rapidly reduced from high temperature, the adatom gas becomes super-saturated resulting in nucleation and the growth of two-dimensional

islands [54]. Diffusion and attachment of the atomic steps on the Si surface also occurs.

The growth of nanowhiskers depends on the cooling rate of the thermal annealing [55]. The fast cooling rate prevents Si adatoms from moving around and freezes them at the position where they are, while they are exposed to the annealing temperature. On the other hand, slow cooling rate allows the Si adatoms to move and have more time to settle down. This leads to more uncertainty for location of those Si adatoms. The growth of nanostructures also depends on thermal adatom concentration. The concentration of "external" and "thermal" adatoms can influence the process of nucleation and growth. Large adatom super-saturation will promote dense nucleation and a small critical nucleus size. In contrast, small adatom super-saturation will promote sparse nucleation and large nucleus size.

2.3.3 Temperature and Duration Dependence

The temperature directly affects the activation energy and hence the growth of nanowhiskers related to the annealing temperature directly. A study in GNS with AFM and SEM investigations have revealed that for annealing temperature between 800°C and 1200°C nanostructure growth was observed on the p-type Si(100), Si(110) and Si(111) surface shown in Figure 2-4 [19]. Their experiments indicate that the nanostructure geometry was found to have nanostructure height ranging between 12nm to 21 nm and existed for all samples annealed within the temperature range 800-1200°C.

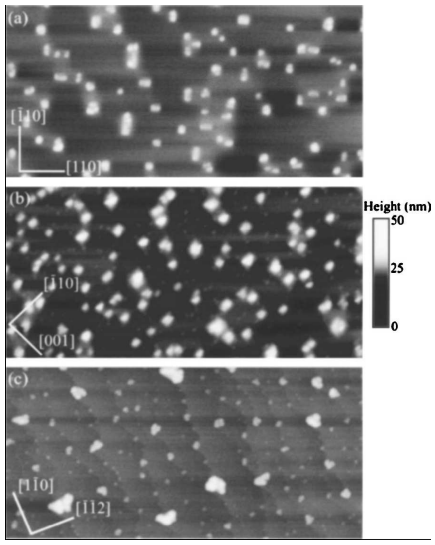


Figure 2-4 4×2-μm^2 plan view AFM image of silicon nanowhiskers formed on silicon substrates by GNS using EB-RTA [19].

The absence of nanowhisker growth under 800°C is due to insufficient void growth. At lower temperatures, there is insufficient activation energy to for the adatoms to overcome the potential barrier on the Si surface. As a result, there are fewer interactions between the Si monomers and oxygen to cause surface disorder. On the other hand, at higher temperature, above 1200°C, the activation energy is high while the potential barrier becomes insignificant, and the adatoms diffusion becomes ineffective. At that high temperature, the evaporation of Si atoms becomes significant and hence the nanostructured surface atoms would be unstable, resulting in atomic scale flattening of the surface and the absence of nanowhisker growth.

The shape of nanowhiskers is dependent on the annealing temperature as the adatom attachment is higher than the rate of SiO_2 decomposition at lower temperature. This is because SiO_2 decomposition was suppressed by the island growth as soon as the islands were created. Therefore the shape of islands is like a hemisphere at low temperature whilst at higher temperature they have pyramidal shape on a Si (100) substrate as the SiO_2 is completely desorbed [56]. The number of islands grown on the Si surface, on the other hand, is proportional to the annealing temperature. At lower temperatures most non-epitaxially grown islands are formed. At higher temperatures, the rest of SiO_2 film on the surface between the pyramidal islands continues to decompose resulting in the production of new surface areas of bare Si.

2.3.4 Density and Annealing Time Duration

The temperature gradients resulted in modifications to the nanostructure geometry as mentioned in the previous section. The annealing duration at a certain annealing temperature is another factor which affects the nanostructure growth. A typical annealing rate profile can be illustrated in Figure 2-5.

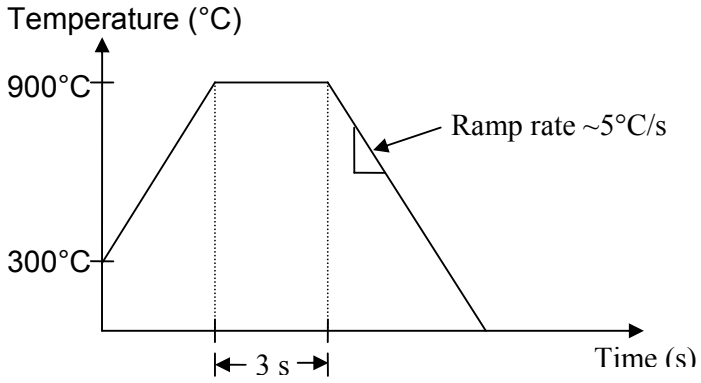


Figure 2-5 A typical annealing time duration at 900°C for 3 seconds.

GNS has studied the nanowhisker growth using the rate at which the samples were heated and cooled was ±5°C/s. From this study, it is clear that the number density of islands up to 30/μm^2 has been observed following annealing at 1100 °C for a duration of 15 seconds as shown in Figure 2-6. However, the island formation in all the annealed samples is independent of the annealing time since all the annealed samples have the same size and number density of nanowhiskers. The height of nanowhiskers, on the other hand, has a linear relationship with the annealing time. The annealing duration and the density have an exponential relationship; the density decays exponentially and then remains constant value of 17.5/μm^2 after annealing for 60 seconds [19]. It has been reported that the annealing duration has no significant effect on the number of nanowhiskers grown on Si surface for annealing duration for 3 seconds to 120 seconds. However, annealing time duration and annealing rate have proportional relationship with the height of the nanowhiskers.

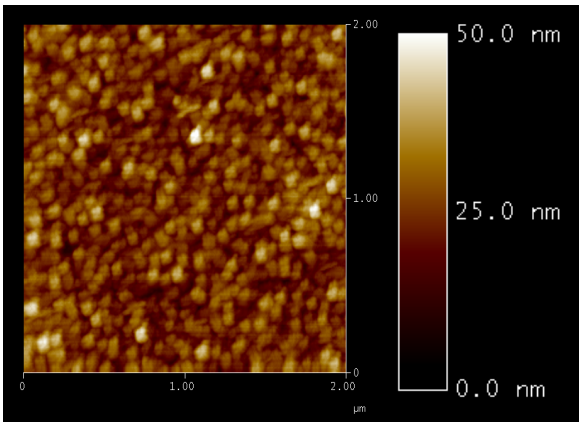


Figure 2-6 Silicon Nanowhiskers from a sample annealed at 1100ºC for 15 s.

2.4 Summary

SOI-SIMOX wafer was chosen to create vacuum microelectronic devices, such as diodes due to its simplicity in fabrication process. To create a useful field emission diode, nanowhiskers were grown on the Si surface acting as the tips for field emission devices. For better understanding, silicon oxidation and mechanism of nanowhiskers growth have been described in this chapter. The silicon oxide and void formation have also been described in this chapter. The reaction between the Si monomers and oxygen can form the voids on the Si surface in controlled annealing temperature, pressure and oxygen concentration conditions. By applying low pressure and low oxygen concentration with high annealing temperature on the Si surface, thermal decomposition can be accomplished. The three-step mechanism was used to explain the void formation and oxide desorption process. These void formation and oxidation desorption mechanism lead to the surface disorder and hence nanowhisker growth on the silicon surface.

The annealing temperatures and annealing duration are directly related as the migration of the Si adatoms is dependent on activation energy which is induced by high temperature. Nanowhisker growth has been observed and revealed that temperatures below 800 °C and above 1200 °C give no nanostructures. The annealing temperature and cooling rate have an effect on nanowhiskers' height and shapes. Higher annealing temperature and faster cooling rate can promote higher

nanowhiskers. However, the annealing duration at a certain temperature has no significant difference in the number of nanowhiskers grown on the Si surface.

The fabrication techniques for field emission diodes using SIMOX nanowhiskers included photolithography, etching, evaporation and metal lift off process; these techniques will be described in the next chapter.

CHAPTER THREE

EXPERIMENTAL TECHNIQUES AND PROCESS

This chapter describes the experimental techniques involved in the fabrication of microelectronic diodes based on nanowhiskers. The main fabrication processes are: diffusion, photolithography, etching, and Rapid Thermal Annealing (RTA). fabrication process of diode structures using SOI wafer is illustrated in Figure 3-1 and described in the following sections.

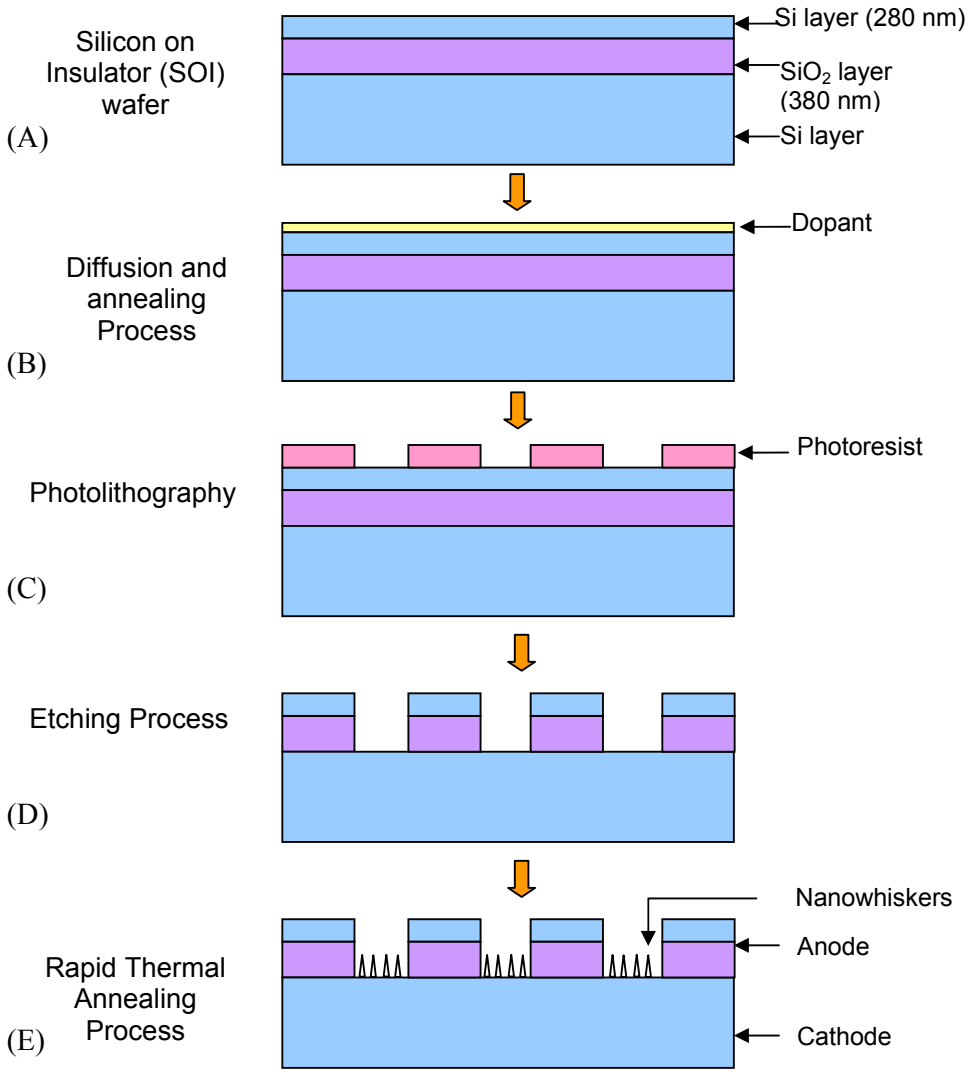


Figure 3-1 Fabrication process for diodes based on silicon nanowhiskers using SOI wafers.

A simple fabrication process is the key for these field emission devices. The objective of this research is to develop an efficient fabrication process for field emission diodes using silicon nanowhiskers as field emitters on the cathode which is the third layer on SIMOX wafer as shown in Figure 3-1. The top-down approach is applied here and hence the RIE and HF etching are required to etch the Si and SiO_2 layers. The fabrication techniques, including diffusion, photolithography, etching techniques, metal evaporation and lift off, electron beam lithography, electron-beam rapid thermal annealing and surface imaging techniques used in this study are described here.

3.1 Diffusion and Annealing Process

Doping via solid-state diffusion is used to make the anode layer in the diode structures highly conductive (Fig. 3-1(B)). Doping or inserting controlled amounts of specific impurity atoms enhances conductivity of a semiconductor sample by increasing either the hole or electron concentration. Dopant atoms can either be "*donors*" or "*acceptors*". Donors donate their valence electrons to silicon so the mobile electron concentration in the silicon is increased, whereas accepters increase the hole concentration. In p-doped silicon, atoms with three valence electrons, group III of the Periodic Table of Element, such as boron, gallium, or aluminium are inserted. In n-doped silicon, atoms with five valence electrons, such as phosphorus, arsenic and antimony are inserted resulting in extra electrons present compared to when all the atoms were silicon. To dope extra electrons or holes into silicon, a diffusion process is commonly used due to its simplicity.

Diffusion can be defined as the motion of particles from high concentration regions to lower concentration regions. Diffusion is used to introduce a controlled amount of dopants into the semiconductor substrate in semiconductor industrial. According to the First Law of Diffusion, the doped atoms penetrate from the high concentration to the low concentration expressed by the following equation [57]:

$$J = -D\frac{\partial C(x,t)}{\partial x} \quad , \tag{3.1}$$

where J is particle flux, C is concentration of solute, D is the diffusion coefficient, x is distance into the substrate and t is diffusion time. With the conservation of mass equation (3.2)

$$\frac{\partial C}{\partial t} = -\frac{\partial J}{\partial x} \tag{3.2}$$

and the First Law of Diffusion, the Second Law of Diffusion known as Fick's Law,

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} \tag{3.3}$$

can be derived having one initial condition and two boundary conditions. These two solutions to Fick's Law are encountered in IC fabrication: constant-source and limited-source diffusion.

3.1.1 Constant-source diffusion

Constant-source diffusion is in which a source of dopants is held at a certain level to ensure that the concentration of dopants at the substrate surface is constant at all time. The initial and boundary conditions are:

$$\begin{aligned} N(x=0,t) &= N_0 \\ N(x>0,t=0) &= 0 \\ N(x\to\infty,t) &= 0 \end{aligned} \tag{3.4}$$

The solution to this type of diffusion under these conditions is as follows

$$N(x,t) = N_0 erfc(\frac{x}{2\sqrt{Dt}}) \tag{3.5}$$

where the error function, *erfc(x)* is defined by;

$$erfc(x) = \frac{2}{\sqrt{\pi}}\int_0^x e^{-t^2}\,dt\,. \tag{3.6}$$

3.1.2 Limited-source diffusion

Limited-source diffusion requires a constant quantity of total dopants per unit area of the diffusion surface which also known as the "drive-in" condition. This means no new dopant is supplied at the surface of the wafer during the diffusion process. The conditions and boundary of this condition are:

$$C(x,0) = 0$$

$$\int C(x,t)dx = S$$

$$C(x,\infty) = 0 \tag{3.7}$$

where, S is the dose. The solution to Fick's Law under these conditions is:

$$C(x,t) = \frac{S}{\sqrt{\pi Dt}} \exp\left[\frac{-x^2}{4Dt}\right] \tag{3.8}$$

In this study, the limited-source diffusion was applied by spinning phosphorosilica films to act as phosphorus source with concentration of $5x10^{20}$ atoms cm^{-3} onto the 1x1 cm^2 samples with the speed of 3000 rpm for 15 s. This phosphorosilicafilm is designed to produce a phosphorus diffused layer in the SIMOX SOI wafer. The silicon layer has extra conduction electrons from phosphorus; hence, this increases the conductivity in the anode. For this particular SIMOX wafer, the diffusion distance should be 280 nm which is where thickness of the upper silicon layer. By applying these equations and the available variables, the diffusion time required to diffuse the phosphorus atoms into the 280 nm depth is 40 minutes (Appendix A).

3.2 Photolithography

Photolithography is process of transferring a mask pattern onto specific areas on the substrate surface. Generally there are six procedures in this process: wafer preparation, photoresist application, soft-baking, mask alignment and UV exposure, developing and hard-baking.

3.2.1 Wafer Preparation

The SIMOX SOI wafer first had to be diced into 1x1cm^2 samples before cleaning. In the semiconductor industry, cleanness is vital thus first step is to remove particulate matter as well as any traces of organic, metallic and ionic contaminants from the

samples. Acetone, methanol and Isopropyl Alcohol (IPA) are commonly used to clean the wafer by immersing it in these chemicals in turn in the ultrasonic bath for two minutes. Then the samples were blown dry with a N_2 gun.

3.2.2 Photoresist application

There are two types of photoresist used in the fabrication process: positive and negative. Positive photoresist is commonly used in IC industry because of its superiority over negative photoresist in terms of controllability for small geometric features, plasma processing operation resistance and quality during development, i.e. they do not swell during development. For positive resists, the resist is exposed to UV light wherever the material is to be removed since the portion of the photoresist that is exposed to UV light becomes soluble to the photoresist developer and the portion of the photoresist that is unexposed remains insoluble to the photoresist developer. The exposed resist is then washed away by the developer solution, leaving windows of bare material underneath. Therefore the mask must have an exact copy of the pattern which is required to remain on the wafer.

On the other hand, negative resist becomes polymerized and more difficult to dissolve when it is exposed to UV light. Thus negative resist remains on the surface where it is exposed, and the developer removes only the unexposed regions. Hence masks used for negative resists have the inverse of the pattern to be transferred.

In this research, positive photoresist (AZ 4620-Clariant Corp.) which can coat the sample up to 1-2 μm thick was applied by spinning at 2000 rpm for 20s and then 4000 rpm for 50s. The first slow speed is applied to achieve the thickest coating as possible and at the same time spread out the resist evenly. The fast-speed spin (4000 rpm) helps to get rid of the excess thick resist at the edge of the samples. The holes of the diode structure are 660 nm deep (top Si layer + SiO_2 layer), accordingly thick photoresist is required to be able to withstand the RIE process for a certain period of time.

3.2.3 Soft-Baking

Soft-baking process is the step where all of the solvents are removed from the photoresist coating. Soft-baking plays a very important role in photo-imaging since

the photoresist becomes photosensitive only after soft-baking. Soft-baking for too long can reduce the photosensitivity of the resists by reducing the developer solubility or destroying some sensitizer. On the other hand, under soft-baking will prevent the light from reaching the sensitizer since there will be some solvent remaining in the coating. This causes incomplete exposure in positive resists. Thus under-baked positive resist is attacked by developer in both exposed and unexposed areas, causing reduced etching resistance. In this research, soft-baking for 20 minutes at 95°C was used to get rid of the excess solvents and dry the photoresist.

3.2.4 Mask Alignment and Exposure

Mask alignment is one the most important steps in photolithography. The mask is a square glass plate with a patterned layer of metal film, such as chrome, on one side. The mask is then aligned with the wafer in order to transfer the pattern onto the wafer surface. This diode structure requires several masks, thus each mask after the first one must be aligned to the previous pattern. After the mask has been aligned accurately with the pattern on the surface, the photoresist is then exposed through the pattern on the mask with high intensity ultraviolet light. There are three common used exposure methods: contact, proximity and projection as shown in Figure 3-2.

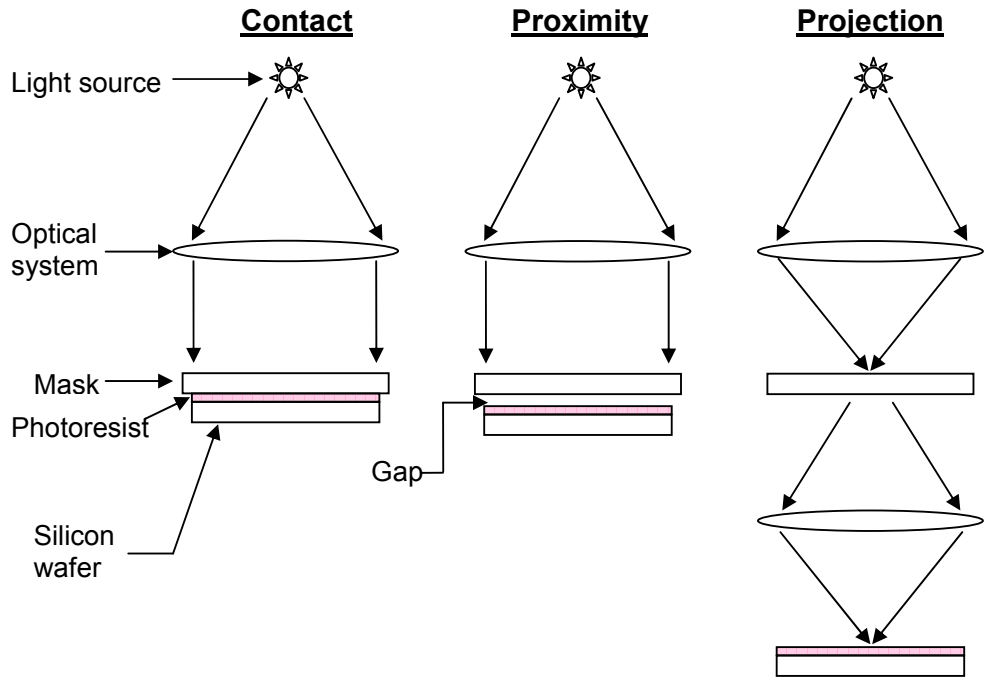
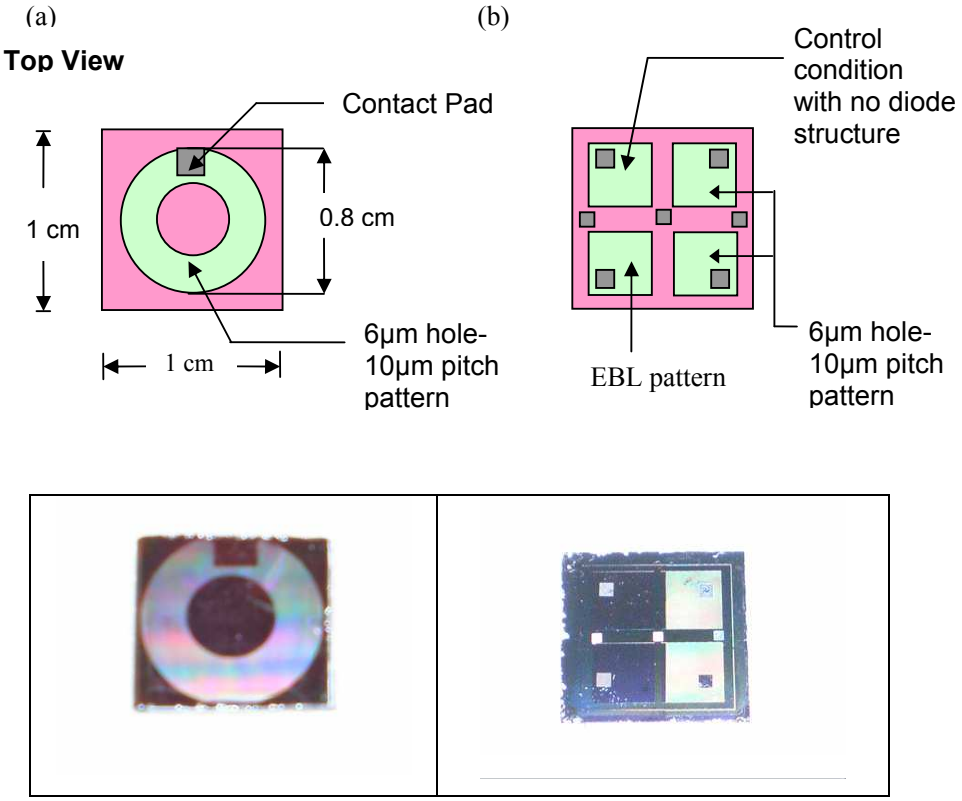


Figure 3-2 Exposure methods in photolithography.

In contact printing, the resist-coated silicon wafer is brought into contact with the metal film side photomask. The wafer, held on by a vacuum chuck, is elevated until it reaches the contact position with the mask. Contact printing has a very high resolution, i.e. 1 μm features in 0.5 μm of positive resist, because of a contact between the wafer and the mask. However, this type of printing has problems with contamination such as debris trapped between the mask and the resist causing defects in the pattern and damage on the mask.

Proximity printing is similar to contact printing except there is a 10 to 25 μm gap between the mask and the resist during exposure. This gap minimizes the mask damage and defects in the pattern but the resolution is reduced to 2- to- 4 μm. Another printing method is projection printing which can eliminate the mask damage entirely. An image of the pattern on the mask is projected onto the resist-coated wafer surface which is a few centimetres away. To achieve higher resolution, only a small portion of the patterns on the mask is imaged. The projection printer that steps the mask over the wafer surface is called a step-and-repeat system. This step-and-repeat system is capable of approximately 1-micron resolution using UV exposure from a mercury lamp, but commercial (and very expensive) deep-UV systems can now achieve resolution to below 100 nm.

The method used in this research was contact printing mode of Karl Suss MA6 mask aligner system by using chrome on glass masks. A mask with 6-μm diameter holes on a 10 μm pitch was used to create diode structures in the shaded area in Figure 3-3. The additional contact masks and a simple 0.8 cm diameter washer were used to create the contact pads and defined area that has diode structures on as shown in Figure 3-3 (a). Later in this research, a more structured device was fabricated using an isolation mask and several contact pad masks as shown in Figure 3-3(b).



(c) An optical image of samples shown in (a) and (b).

Figure 3-3 Top view of the samples with diode structures (a) with the washer as a mask and (b) with four isolation areas.

3.2.5 Development

Development is the process that removes the soluble resist on the wafer surface after exposure to ultraviolet light. The exposed regions of negative resist remain after development as the exposure energy is increased above the threshold energy (E_t). In positive resists, the resist becomes more soluble in the developer when it is exposed to ultraviolet light at some threshold energy level. Nevertheless, the quality of the developed pattern depends on various variables, such as the initial resist thickness, prebake conditions, developer chemistry and developing time. The developer used in this study is AZ 300 MIF (Clariant Corp.). After a few test experiments, the best developing time for this diode structure pattern was determined to be 2 minutes at 23°C.

3.2.6 Hard-Baking

Hard-baking process is the final step of photolithographic process which the images are thermally treated to improve their resistance to a subsequent process. The higher temperature, 120 °C ~ 185° C region, improves the adhesion to the substrate and the resistance to etchants. However, another factor that must be considered is that the reflow of the photoresist would have opposed influence on the photoresist profiles. Consequently, hard bake temperature and time were trade off between resist profile and resistance to RIE process. The final hard baking conditions were 185° C for 15 minutes.

3.3 Etching Process

Generally there are two classes of etching processes for etching thin films to form microelectronic structures. Dry etching such as RIE, sputtering etching and vapour phase etching involves both physical and chemical reactions where the material is dissolved using reactive ions or a vapour phase etchant. Wet etching is where material is dissolved when immersed in a chemical solution. The most common technologies for wet and dry etching will be briefly discussed here.

3.3.1 Reactive Ion Etching Process

The Reactive Ion Etching (RIE) process is one of the most common uses of a combination of chemical and physical processes. It uses the principle of bombarding the material to be etched with highly energetic chemically reactive ions. The chemical part of the process is where reactive particles are ionised in the plasma when a gas is subjected to a DC or Radio Frequency (RF) potential at reduced pressure. Then they are accelerated to the electrode surfaces within the discharge chamber. Figure 3-4 illustrates the typical RIE process.

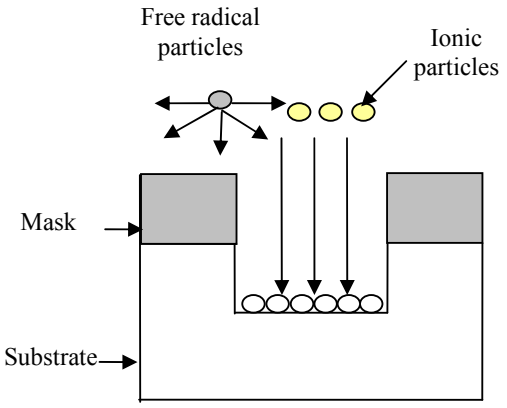


Figure 3-4 A diagram of ionised charges bombarding a masked substrate in a reactive ion etching process.

The ionized charges bombard the substrate surface where the mask material such as photoresist and metal are not present creating the profile according to the patterns on the mask. At low pressure, this type of etching can achieve highly anisotropic results with vertical sidewalls. For this research, both silicon and silicon dioxide layers are required to be etched to create diode structures as shown in Figure 3-5.

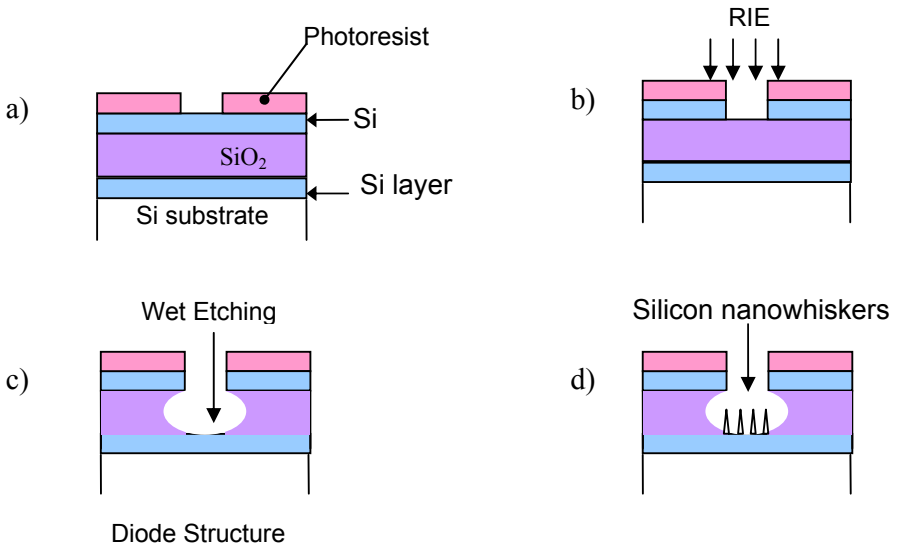
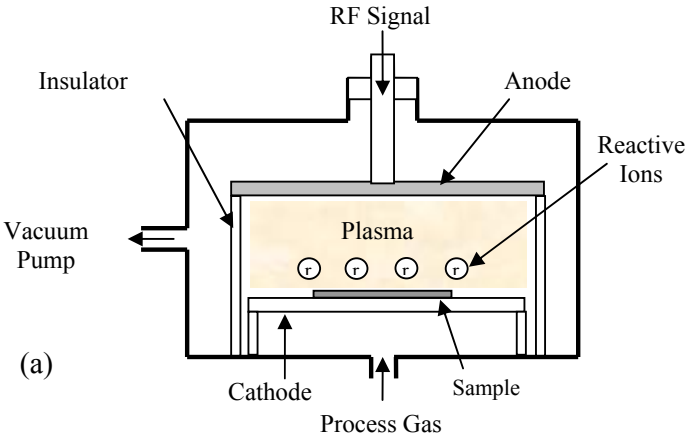


Figure 3-5 Diode structures was created using Reactive Ion Etching (RIE) and wet etching processes.

An Oxford Plasma Lab 80 Plus, dry etching system, shown in Figure 3.6 was used for this research. The first layer of silicon to be etched has the thickness of 280 nm. To etch the required thickness of silicon, a Sulphur Hexafluoride/Oxygen (SF_6/O_2) gas mixture recipe was used. This process was carried out at a temperature of 295 K, with the pressure of 7 mTorr, gas flow rates 90 sccm/ 5 sccm, RF power of 150 W and time of 3 minutes. The second layer is 380 nm thick of silicon dioxide (SiO_2) layer. Initially a dry etching process was performed to etch only a third of SiO_2 layer down ensuring the vertical sidewall. This layer of SiO_2 was etched using a gas mixture of a Halocarbon 23/Argon (CHF_3/Ar) at temperature 295 K, with the process pressure of 3 mTorr, gas flow rate 25 sccm/ 30 sccm, RF power of 200 W and an etching time of 3 minutes. These RIE conditions were chosen using pre-determined recipes [58] and finalised by some experimentation. Finally, wet etching process using Hydrofluoric acid (HF) was used to achieve an undercut profile in the SiO_2 layer.



b)

Figure 3-6 (a) A schematic of typical parallel plate reactive ion etching system, and (b) Oxford Plasma Lab 80 Plus system used in this study.

3.3.2 Wet Etching Process

Wet etching is used to remove unwanted layers of material by immersing the sample in a liquid bath of chemical etchant. There are two types of wet etchants: isotropic etchants and anisotropic etchants. The isotropic etchants etch the material at the same rate in all directions whilst anisotropic etchants attack the material at different rates in different crystal directions. Hence the isotropic process promotes undercut sidewall profiles. In this research the undercut profile is required to prevent the short circuit between the top Si layer and the nanowhiskers as illustrated in Figure 3-4. Hydrofluoric (HF) acid is used to etch silicon dioxide, SiO_2, due to its high selectivity over silicon where the etch rate of SiO_2 is much higher than the etch rate of Si. HF can easily be masked by photoresist and the etch rate is relatively repeatable even after a large numbers of samples have been etched.

The etchant used for this purpose was buffered HF, NH_4F: HF (7:1) which has the etch rate of approximately 100 nm/min at room temperature, [59]. The addition of ammonium fluoride (NH_4F) to HF controls the pH value and replenishes the depletion of the fluoride ions, therefore maintaining the stable etch rate. The chemical reaction of this etching can be shown as following:

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O. \quad (3.9)$$

For this study, the HF etching takes only 110 s to etch through the SiO_2 layer. After HF etching the samples were immersed in DI water for a minute to stop the etching reaction.

3.4 Metal deposition and Lift Off

The thin metal film used as contact pads was deposited onto the back of the sample and onto the contact area of the front side of the sample by using a metal evaporator, shown in Figure 3-7. The fundamental operation of metal evaporation is to deposit a thin metal film all over the sample, covering areas with or without photoresist. For the process described here, a 40 nm thick Aluminium layer was deposited on the back of the sample for a cathode contact pad. Later in the research, a 40 nm thick

Nichrome (NiCr) was deposited onto the sample surface which has uncovered area of resist at the contact pads. NiCr serves the required properties of robust masking material during RIE and has reasonable electrical conductivity to be used as a contact pad.

After evaporation, the samples were immersed in acetone for several hours to lift off the NiCr in every area except the contact pads to complete metal lift off process. During this process, NiCr on top of resist layer was removed together with resist by acetone, while the NiCr film deposited directly on the substrate remained unaffected.

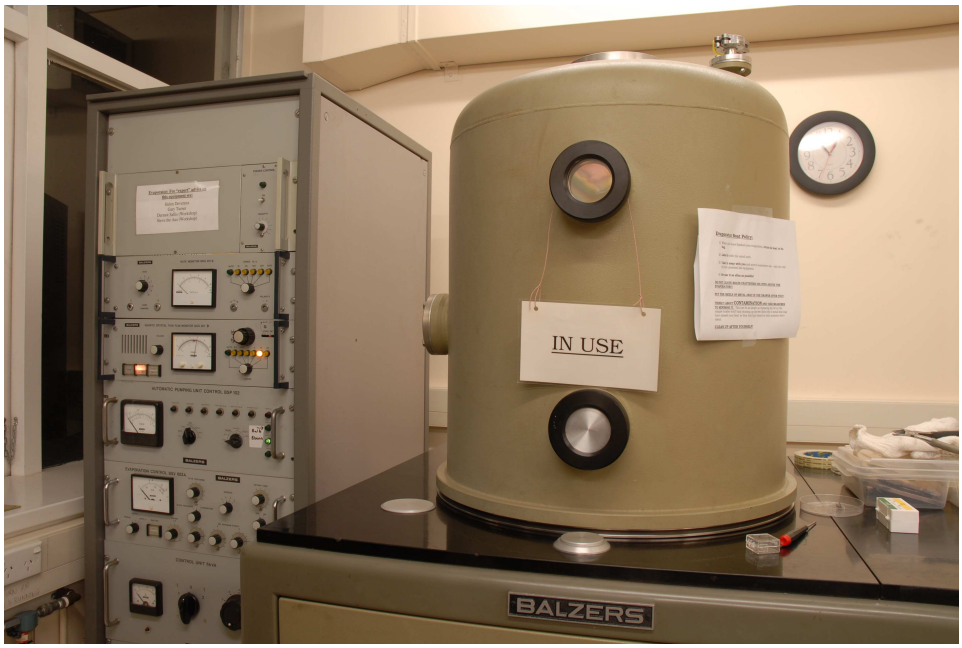


Figure 3-7 Metal Evaporator system with the controller on the left and the vacuum chamber on the right.

3.5 Electron Beam Rapid Thermal Annealing (EB-RTA)

Rapid Thermal Annealing (RTA) is a process commonly used in semiconductor industry in an environment from ultra high vacuum to ambient pressure with different atmospheres, such as oxygen and nitrogen. Electron Beam Rapid Thermal Annealing (EB-RTA) is the RTA system which uses an electron beam as the source of energy based on the collisions of electrons and the sample. A common EB-RTA system can

heat up the samples to temperatures between 300°C and 1200°C in the presence of different gasses. A schematic diagram of the EB-RTA system at GNS Sciences is shown in Figure 3-8; this allows the user to control program functions via a controller keyboard to obtain silicidations, anneals and other applications that require high temperatures in short period of time.

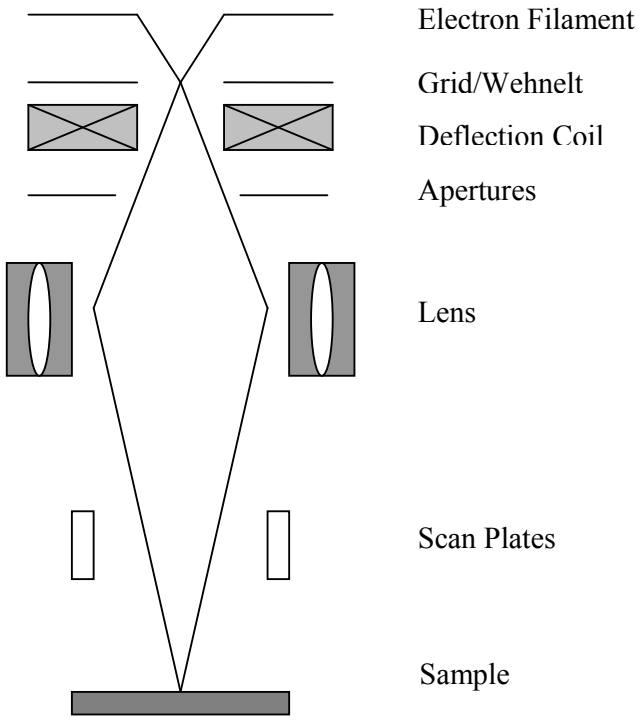
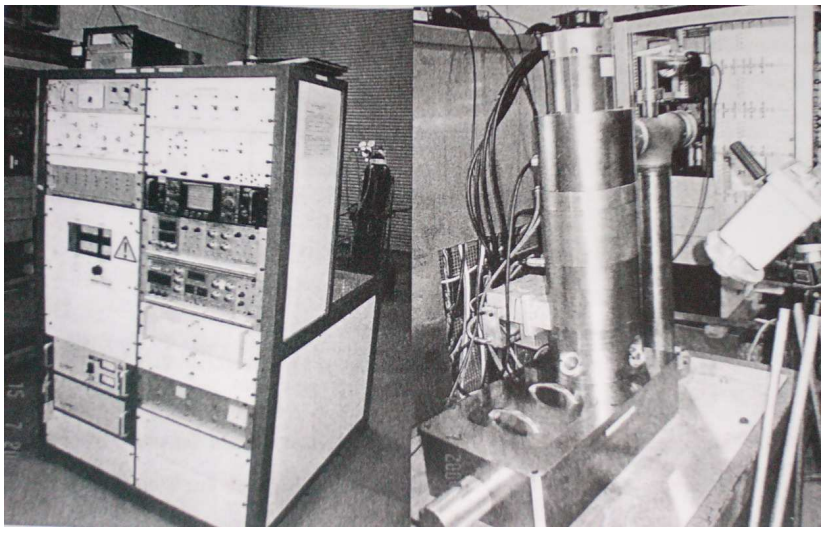


Figure 3-8 Schematic diagram of vacuum chamber of Electron-Beam Rapid Thermal Annealer.

The annealer consists of high-intensity electron filament which is contained in cooled reflective walls, grid/wehnelt electrodes, deflection coils, apertures, lens and scan plates. The deflection coil is used to adjust the electron beam before it is condensed by the lens. After the deflection and focusing system, the electron beam is precisely scanned on specific locations by scan plates and hence energy is absorbed by the sample causing high temperature at the sample surface. Figure 3-9 shows the EB-RTA system at GNS Sciences with the vacuum chamber and the control unit.



(a) (b)

Figure 3-9 EB-RTA system at GNS Sciences (a) control system, and (b) vacuum chamber system [59].

The annealing profile is manipulated by controlling the electron beam intensity. The temperature of the sample surface is monitored by an optical pyrometer connected to the feedback loop of the controller. This pyrometer can determine the temperature by the colour of the sample surface and can also send this to the plotter to print out a hard copy of the temperature profile. The EB-RTA system is not only able to precisely control the annealing temperature and pressure, but also control the rate of heating up and cooling down, which is vital in the thermal annealing process for nanowhiskers' growth. However contamination on the pyrometer probe such as photo resist, carbon deposits produced by oil from the vacuum system and low melting point metal affects the accuracy of the temperature reading. Therefore sample coating materials are needed to be considered to prevent contamination.

3.6 Electron Beam Lithography

Electron Beam Lithography (EBL) was used to create different-size patterns for diode structures directly on resist coated substrates without any optical mask. A Raith 150 system with a LEO 1500 series scanning electron microscope as a core was used for this research. Electron beam lithography gives high-resolution results because of its thermal-field-emission electron source [60]. This Raith 150 system has a range of beam-acceleration voltage from 200V to 30kV, and working distance from 20 mm to less than 1 mm. The basic principle of EBL is similar to photolithography; the electron beam acts as an exposure source and different type of resists can be used. The electron-beam resist is coated on the surface and the electron beam can then be used to write the pattern directly on the resist surface. Positive electron-beam resists dissolve in the developer because electrons cause scission of polymer chains in the resists. The electron-beam resist used in this research is a single layer of 996 K-molecular-weight polymethyl methacrylate (PMMA), 8% solution in Xylene.

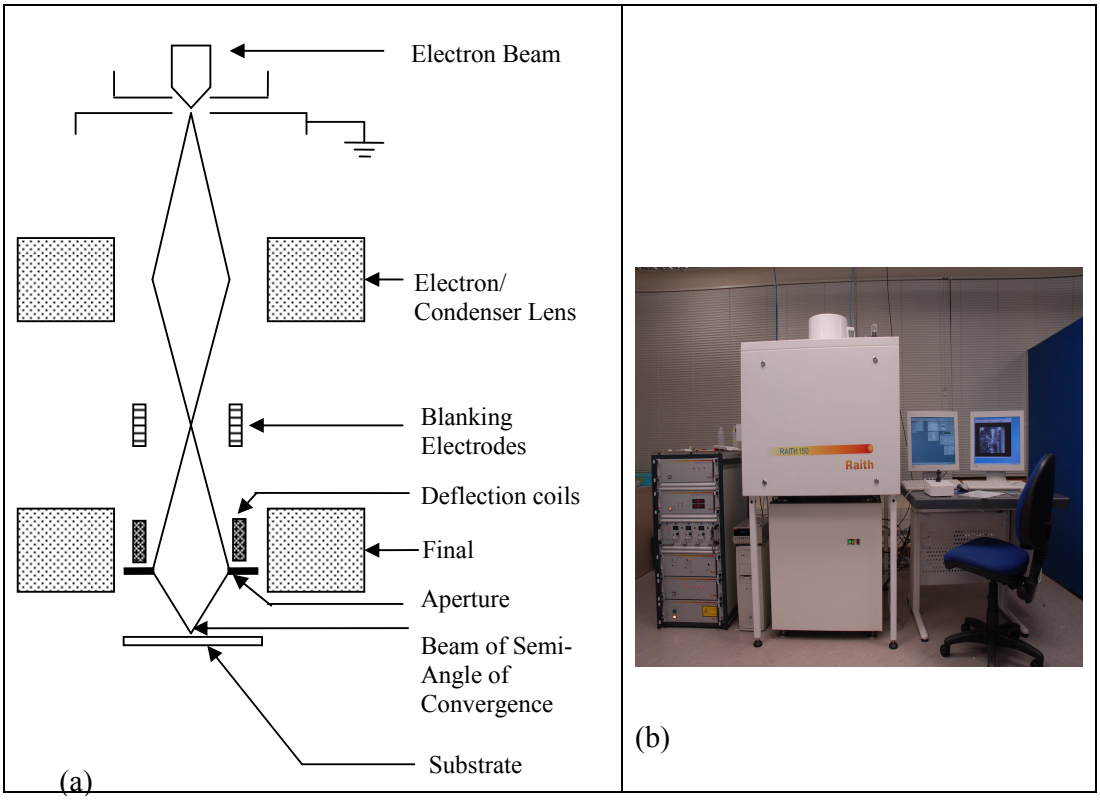


Figure 3-10 (a) A schematic view of Electron Beam Lithography (EBL) system and (b) a Raith 150 system with a LEO 1500 series used in this research.

Figure 3-10 shows a schematic view of a typical Electron Beam Lithography (EBL) system that used in this research to create different features on the samples. The electron beam can be generated using a number of different sources, for example cold Schottky emitters for field-emission systems, tungsten (W) and lanthanum hexaboride (LaB_6) for thermionic emitters. Then the electrons are accelerated by electrostatic fields to energies from a few keV up to 200 keV. The condenser lenses and beam aperture are used to narrow and focus the beam. The beam blanker is used to turn the electron beam on and off rapidly according to the desired patterns.

There are two PMMA resists for electron beam lithography available; Low Molecular Weight (LMW, 120 kg/mol) and High Molecular Weight (HMW, 996 kg/mol). To prepare these PMMA resist solutions, two types of solvent were used. LMW PMMA was dissolved in chlorobenzene and HMW PMMA was dissolved in Xylene. The PMMA resist used in this research was 8% HMW PMMA to achieve a thick coating layer on the sample. It is used to ensure that it can withstand a few minutes of the RIE process.

3.7 Imaging of Surface Topology

Various techniques of imaging surface and nanostructures are available but the most common ones are atomic force microscopy (AFM) and scanning electron microscopy (SEM). A very high resolution image is achievable using these techniques. However, SEM has some disadvantages because it is expensive to purchase the electron beam system and maintain.

3.7.1 Atomic Force Microscopy (AFM)

Atomic Force Microscopy is one of the most common surface scanning tools providing high-resolution images of various surface properties. AFM uses a sharp probe or tip to measure a local property, such as height, optical absorption, or magnetism by placing it very close to the sample surface. The schematic of an AFM system is shown in Figure 3-11(a). AFM measures either attractive or repulsive forces between a tip and the sample [61]. In its repulsive or “contact” mode, the apparatus touches a tip at the end of cantilever to the sample and the tip dragged over

the sample surface in raster scan. In contact mode the AFM measures hard-sphere repulsion forces between the tip and sample.

In this research, a Digital Instruments Dimension 3100 AFM system, as shown in Figure 3-11(b), was used in tapping mode with common type of non-contact tip, NSC 11/50 (Micromasch Corp.) which operates by scanning a tip attached to the end of oscillating cantilever across the sample surface. This cantilever is oscillated at near resonance frequency with amplitude ranging from 20nm to 100nm [62]. The feedback loop maintains the constant oscillation amplitude by maintaining constant RMS of the oscillation signal acquired by the split photodiode detector. The tip-surface interaction is monitored by reflecting the laser beam of the back of the cantilever into a split photodiode detector. By detecting the difference of in the photodetector output voltages, changes in the cantilever oscillation amplitude are determined. The topographic image of the sample surface is formed using vertical position of the scanner at each (*x,y*) data point [61].

AFM can also provide useful surface analysis such as particle analysis, roughness analysis and section analysis. Particle analysis was used to determine number of nanowhiskers grown on the surface within a specific area and its density. The dimension of the diode structure was measured by using section analysis, and results are shown in chapter 4.

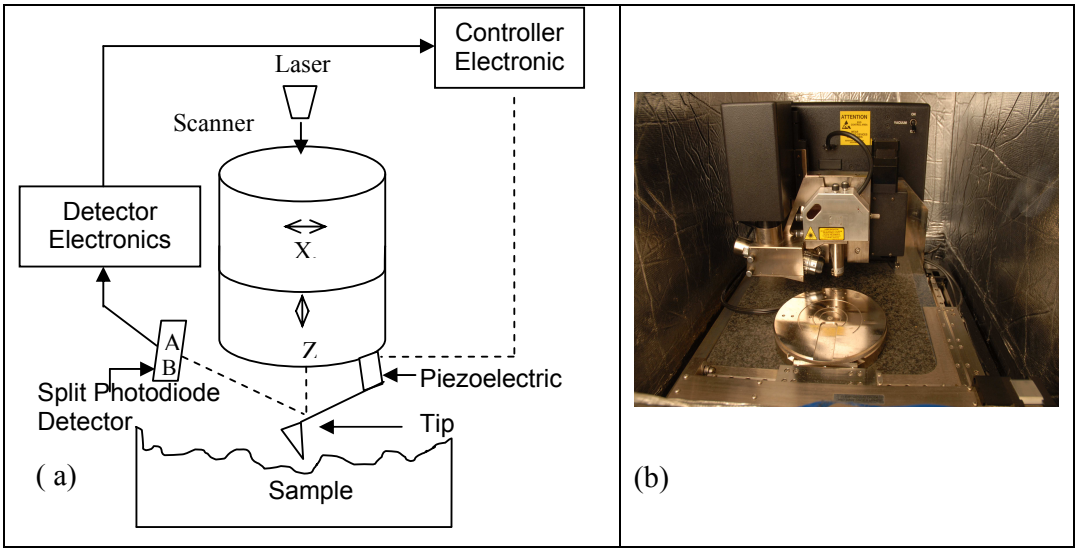


Figure 3-11 (a) A schematic view of Atomic Force Microscopy (AFM) and (b) AFM system with digital instrument, Nanoscope IIIa.

3.7.2 Scanning Electron Microscopy (SEM)

The fundamental operation of SEM is similar to the EBL shown in Figure 3.8. The electron beam produces images by detecting secondary electrons which are emitted from the surface due to excitation by the primary electron beam [62]. In the SEM, the electron beam is scanned across the sample in raster mode, with detectors building up an image by mapping the detected signals with beam position. SEM images of diode structures were obtained and are illustrated in chapter 4. The cross section of the diode structure was also obtained to evaluate the undercut sidewall of the SiO_2 layer.

3.8 Summary

Field emission diodes using SIMOX wafer were produced by the simple fabrication process discussed earlier. The two main parts of this process are: diode structure fabrication and nanowhisker growth. These diode structures were achieved using photolithography, EBL and etching techniques. This chapter described the principle behind each fabrication step and how they could be applied in this research. In the next chapter, the results of the fabrication process, together with the surface and electrical characteristics of these field emission diodes will be discussed in detail.

CHAPTER FOUR

EXPERIMENTS AND RESULTS

The samples with diode structures produced by using photolithography and etching processes mentioned in the previous chapter were sent to grow nanowhiskers on the Si surface at GNS. With a precise temperature and electron beam intensity control of the RTA system, nanowhiskers have been grown with different temperatures and annealing times. In order to investigate nanowhisker growth pattern and density for different annealing temperatures and times, several experiments were performed to achieve the best possible conditions for growing nanowhiskers on the underlying Si layer of the SIMOX-SOI wafer; this is a surface that has not been used for nanowhisker growth previously, hence the need for this fundamental characterisation. The following sections will describe the fabrication process development, the actual physical sizes and appearances of the nanowhiskers, and field emission properties that have been observed.

4.1 Fabrication Process Development

The objective of this fabrication process is to produce a complete field emission device with the simplest possible method. First the diffusion time for doping the anode layer was calculated according to the required distance into the substrate as discussed in Chapter 3. The suitable field emission electrode structure, UV exposure time, developing time, RIE process recipe and HF etching time were also considered to obtain the required diode structures and the results are presented here.

4.1.1 Electrode Structure Design

The primary component of any field emission display is the cold cathode. This structure must be able to emit electrons at low macroscopic electric fields (typically in the range 1-20 $V\mu m^{-1}$) with sufficient current density (typically in the range 10-100 $mAcm^{-2}$) to generate bright fluorescence from the associated phosphor on the anode

[63]. The common electrode structures used in the field emission industry are diodes and triodes. However, diodes are generally easier and cheaper to produce than triode devices mainly because of the time consuming and equipment-demanding nature of field emission device fabrication. Therefore, in this study diode structures were chosen as mentioned previously and as shown in Figure 4-1. Figure 4-1 (a) is a simple diode structure pattern that is designed to test the field emission characteristics of the micro-scaled diode structures. Several sizes of diode structures were created by EBL to investigate the effects of feature size on the field emission characteristics, using a set of samples as shown in Figure 4-1 (b). The decreasing in feature size is likely to have some effect on the emission current as well as the edge effect where field emission is likely to be stronger at the edge than the top of the gate [64]. It is also important to investigate the effect of the distance between the emitters to the emission current. The emitter density is assumed to be increased if the gate-hole size is decreased. The decreased in distance between emitters may induce a screening effect of the nearby emitters.

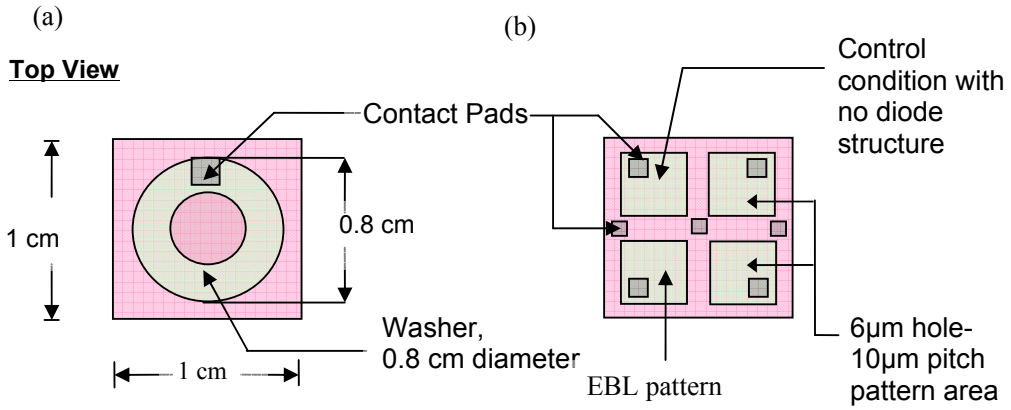


Figure 4-1 Diode structures use (a) the 0.8 cm diameter washer and (b) 4-isolation mask.

The samples shown in Figure 4-1(a) used a washer with 0.8 cm diameter as an optical mask, due to its robustness, cost and availability; this allowed a pattern of 6-μm holes to be created inside the defined washer area. This leaves a space outside the washer area to be etched down to the cathode layer. The flood exposure was used to expose the whole sample without using an optical mask that is in vacuum contact to the sample surface. Later, more detailed optical masks (Fig.4-1(b)) were developed by

using L-Edit program to draw a schematic view of the desired patterns which was then printed on a transparent sheet with a high-resolution printer. The mask pattern was then transferred to a nichrome-on-glass mask using the basic photolithography techniques. Within the washer area (Fig. 4-1 (a)) and the four-isolation area (Fig.4-1(b)), the contact pads are required for the electrical connections at the anode layer for the electrical measurements.

4.1.2 UV Exposure Time

To form the different patterns a high-pressure mercury arc UV light source was used to expose the samples. The exposure time required to expose the 1-2 μm thick layer of the positive photoresist AZ 4620 was determined via two experiments testing different flood exposure times as presented in Table 4-1 and Table 4-2. Flood exposure is required for get rid of the unwanted areas outside the mask (i.e. washer) as shown in Figure 4-1 (a). After developing for 2 minutes, the area outside the washer was observed using the microscope resulting in the optimum flood exposure time of 180 s.

Table 4-1 Optimum flood exposure time experiments

Samples	Flood Exposure Time (s)	Areas with remaining photoresist after 2mins of developing		
		Outside mask	Masked area	Remarks
1	160	Yes	Yes	Thick layer in both areas
2	165	Yes	Yes	Thin layer outside the mask
3	170	Yes	Yes	Thin layer outside the mask
4	175	Yes	Yes	Residue outside the mask
5	180	No	Yes	No residue in non-image area
6	185	No	No	Image area has been peeled off

The flood exposure and hard-contact exposures are supposed to be carried out consecutively before developing. Similarly, the vacuum exposure time was determined providing that samples had undergone 180 s of flood exposure previously. The results of different vacuum exposure times using the 6 μm diameter holes on 10 μm period are illustrated in Table 4-2.

Table 4-2 The optimum vacuum Exposure time testing.

Sample	Vacuum Exposure Time (s)	Areas with remaining photoresist		
		Outside washer	In the 6 μm holes	On the image pattern
1.	80	Yes	Yes	Yes
2.	85	No	Yes	Yes
3.	90	No	No	Yes
4.	95	No	No	Yes
5.	100	No	No	Yes, with enlarged holes
6.	105	No	No	Yes, with partially removed pattern

In conclusion, the optimum UV exposure times are flood exposure for 180s and followed by the 90 s with hard-contact exposure. In some occasions, these exposure times have to be adjusted, due to the different thickness of applied photoresists. When the photoresist gets thicker, the same spin speed and time will result in a thicker photoresist layer. However, this procedure is reasonably reliable judging from the fact that at least 90% success rate was obtained in each set of samples.

4.1.3 Developing Time

Developing is the process of removing the unwanted photoresist from the samples using AZ 300MIF a base solution (2.38% TMAH Clariant Corp.). As discussed in Chapter 3, the resist becomes more soluble in the developer when it is exposed to ultraviolet light at some threshold energy level for the positive photoresist. The concentration for the developer and the temperature were fixed in advance to decrease the uncertainty in the process. The developing time is the only parameter for optimizing the developing process. The primary requirement of development time was complete residue-free removal of the non-imaged resist. This means the developing time must be long enough to prevent underdevelopment, in which the residue remains around the fine pattern. In contrast, if the developing time is too long,

overdevelopment will change the geometry of the patterns, even causing the patterns to be peeled off. It was also noticed that the slope around the edges of the patterns changed with long exposure time. Therefore, developing time of 2 minutes was finally fixed, which also made it possible to develop the pattern precisely. After development, the samples were rinsing by immersion in DI water then dried using dry nitrogen.

4.1.4 Reactive Ion Etching Process

The Si and SiO_2 layers have to be etched to create the diode structures as shown in Figure 3-5. The general requirements of RIE of Si and SiO_2 layers are presented in Table 4-3. Among the requirements, etch rate, selectivity and uniformity are general RIE requirements. Low etch rate gives rise to long etch time, thus process instability could occur. Low selectivity would lead to a sloped profile, while poor uniformity could result in poor etch depth control. The reason to etch only 100 nm of SiO_2 with RIE is that the rest of the SiO_2 layer can be etched by using HF etch to give the desired undercut. This 100 nm depth of SiO_2 was required to ensure that the top layer of SiO_2 was etched, instead of the Si layer on top of the sample.

Table 4-3 The requirements for RIE of Si and SiO_2 layer.

Items	Requirements	
	Si Layer	SiO_2 layer
Etch rate (nm/min)	>50	>20
Etch depth (nm)	280	180
Selectivity to photoresist mask	>10	>10
Etch uniformity	<5%	<5%
Side wall angle (°)	90 ± 5	90 ± 10

By following the general recommended RIE conditions for Si etching, the RIE conditions were then fixed and leaving only the etching time as a variable. Trials were performed to achieve the Si layer etch requirements using the conditions, including gases, flow rates, RF power, pressure, temperature and etch time shown in Table 4-4.

Table 4-4 The RIE conditions for Si and SiO_2 layer etch.

Parameters	Conditions	
	Si layer	SiO_2 Layer
Feed gases	SF_6/O_2	CHF_3/Ar
Flow rates	90 sccm/ 5sccm	25 sccm/ 30 sccm
RF Power	150 W	200 W
Etch Pressure	7 m Torr	3 m Torr
Temperature	295 K	295
Etch Time	3 mins	4 mins

The RIE conditions shown above provide a vertical sidewall profile of Si and SiO_2 layer as required. However, for the longer etch time of the Si layer, such as 6 mins, the sidewall appears to be a sloped profile, which is undesirable. Wet etching was then applied to etch the remaining 200-nm thick SiO_2 layer. This will be discussed in the next section.

4.1.5 HF Etch

As already discussed in details of the HF etch principle, this section presents the HF etch time experiments. From the previous section, RIE was used to etch the first 100 nm of SiO_2 and then the buffered HF solution, NH_4F: HF (7:1) which has the etch rate of approximately 100nm/min at room temperature, was used to etch the remaining 200 nm. Therefore, HF etch times ranging from 100 s to 120 s were tested. The results turned out that 110 s of HF etch etched the SiO_2 layer to the required depth. The AFM images of diode structures that have been etched using the conditions in Table 4-4 and followed by HF etch for 100 s, 110 s and 120 s, respectively are illustrated in Figure 4-2.

To see the undercut sidewall required to prevent the electrical bypass between the cathode emitter and the anode, SEM images of the cross section of the samples can be obtained because the AFM system has no capability of detecting any undercut profile. As can be seen in Figure 4-2, every image structure has vertical sidewalls. The sloped profile observed in Figure 4-2 (e) and (f) shows that if the HF etching is too long, over

etching at the edge of the features may occur and may cause poor electrical contact at the anode. Unsurprisingly, the longer HF etching time promotes deeper diode structures, in particular after 120 s of HF etching the diode structures have been etched to 692 nm as shown in Figure 4-2 (f). Regarding this experimental results, the best HF etching time is 110 s, which etches the SiO_2 to the required depth of 660 nm as shown in Figure 4-2 (d).

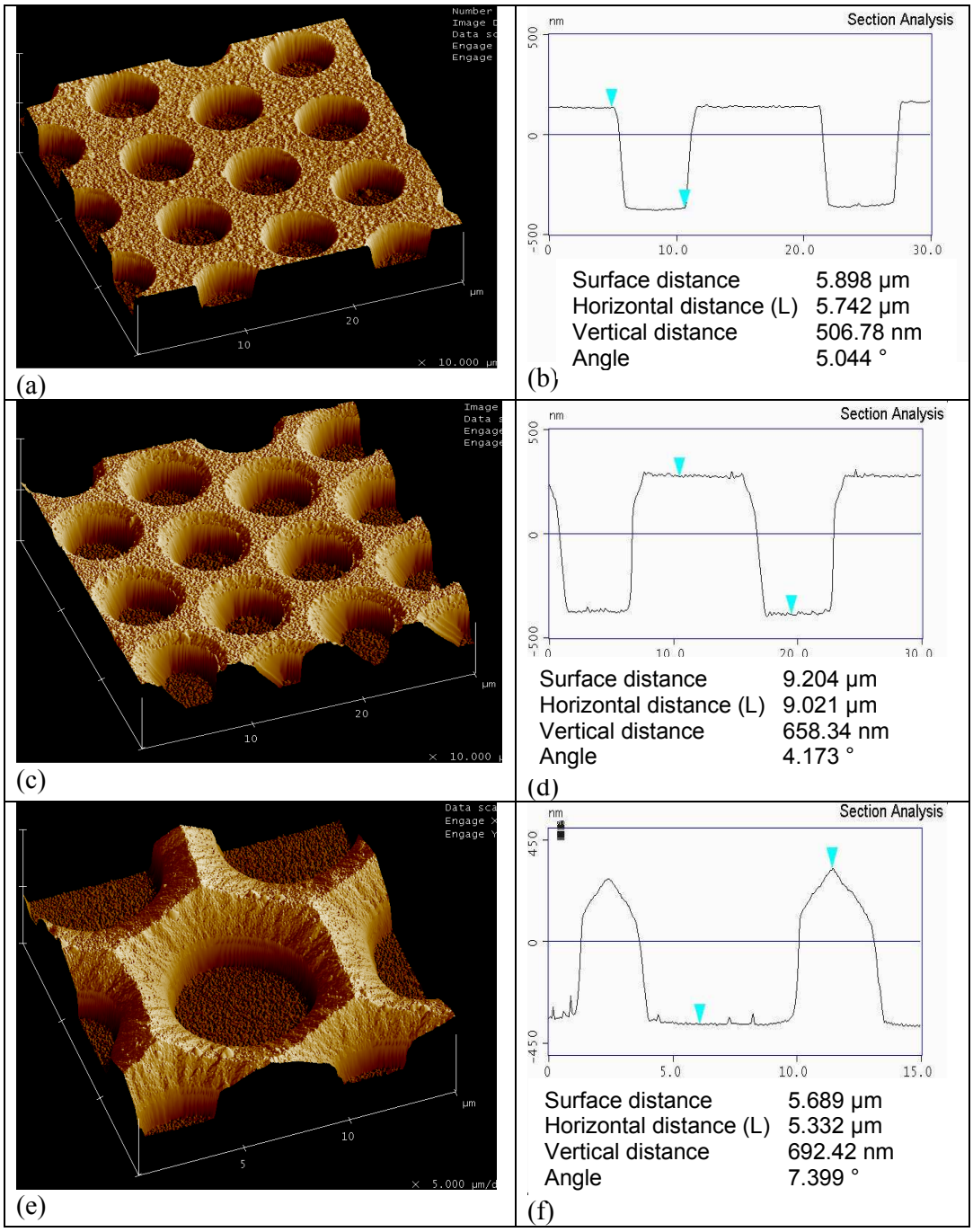


Figure 4-2 AFM images and their section analysis showing the different depth of structures etched by using conditions in Table 4-4 and followed by HF etch for (a) 100 s, (b) 120 s and (c) 130 s.

4.1.6 PMMA Coating and EBL Patterning of EBL-formed Structure

The structures shown in Figure 4-1 (b) were created using EBL patterning methods to achieve different feature size diode structures. The first process is resist preparation. As mentioned in Chapter 2, the electron beam resist, 8% PMMA, was used in this study as a mask in RIE and HF etch. The resist was spun onto the samples at 3000 rpm for 1 minute. To cure the PMMA, soft baking on a 170 ºC hotplate for 90 s is required.

A set of samples were produced to test the effect of different feature sizes on the field emission. To create the different feature sizes, EBL system was used to write the 2 μm-feature-on-5 μm period, 5μm-feature-on-10 μm period and 10 μm-feature-on-50 μm period patterns. Before writing the EBL patterns, the suitable areal dose that is enough to break sufficient molecular bonds of this PMMA solution was determined by writing an array of features with different area dose ranging from 72 $\mu As/cm^2$ up to 336 $\mu As/cm^2$. It turned out that the area dose of 216 $\mu As/cm^2$ was the optimum value. The conditions for writing these EBL patterns are presented in Table 4-5.

Table 4-5 The EBL condition for creating EBL patterns.

Parameters	Conditions
1. Area dose	216 $\mu As/cm^2$
2. Voltage	10 kV
3. Electron beam aperture	30 mm
4. Area step size	20 nm

After the EBL patterning, the samples were developed by immersion in MIBK:IPA, 1:3, developer for 1 minute and then followed by RIE and HF etch using conditions shown in Table 4-4. The diode structures and surface characteristics of these devices will be discussed in Section 4.5.

4.1.7 Fabrication Procedure

The fabrication procedure of the diode structures using many procedures, such as sample preparation, photoresist coating, soft baking, UV exposure, hard baking, RIE etching and wet etching can be illustrated in a simple diagram shown in Figure 4-3.

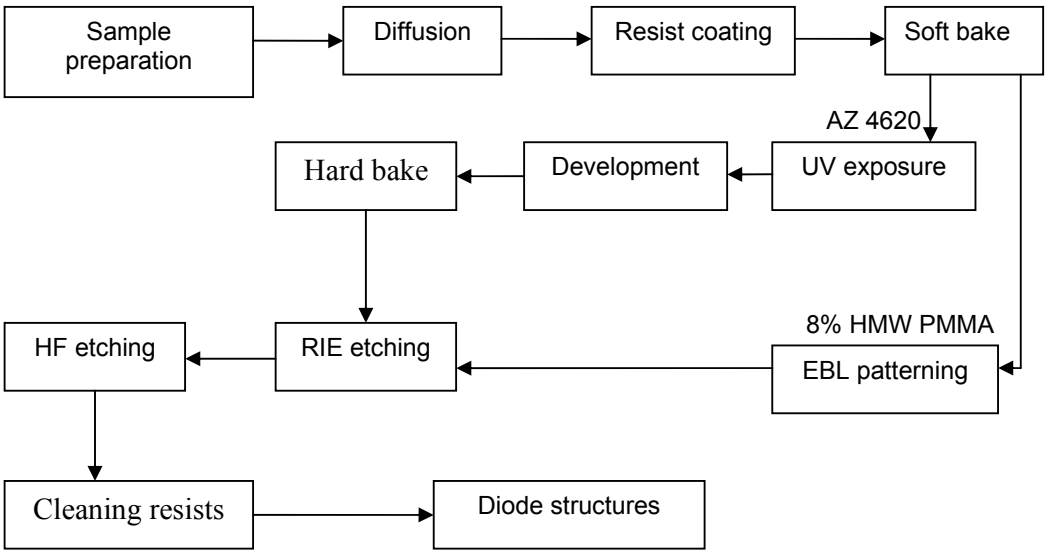


Figure 4-3 The fabrication procedure of the diode structures.

Sample preparation and diffusion conditions are the same for both methods. The first step is to dice the SIMOX wafer into 1 × 1 cm samples using the wafer scriber. Then the samples were cleaned using acetone, methanol and IPA respectively for 2 minutes each time. After 15 minutes baking at 95 °C to dry the excess solvents, the phosphorosilica film with $5x10^{20}$ atoms cm^{-3} was spun at 3000 rpm for 15 s onto the samples. Before the diffusion process, the samples were baked at 185 ºC for 15 minutes to get rid of the solvent. The 1000 °C furnace with air atmosphere was required to diffuse more dopants into the anode layer for 40 minutes. Then positive photoresist (AZ 4620-Clariant Corp.) was spun onto the samples with a two-step speed of 2000 rpm for 20 s and 4000 rpm for 50 s for the 6 μm-hole-pattern structures. To remove the solvent and increase the adhesion of the photoresist before exposure to the UV light, the samples were baked at 95 °C for 20 minutes. Two-step exposure was required to expose the photoresist layer to create not only the washer isolation, but also the 6 μm diameter holes on a 10 μm pitch on the samples. The flood

exposure of 180 s was required to expose this thick photoresist using the washer mask on top of the sample surface. Then the vacuum exposure mode was applied to expose non-feature area with the UV light for 90 s. The samples were then developed for 2 minutes using AZ 300 MIF developer to get rid of the photoresist in the unwanted areas. Hard baking at 185 °C for 30 minutes was required to dry the excess developer and make the photoresist able to withstand the RIE and HF ecthing with conditions discussed previously.

On another set of samples, the 8% HMW PMMA was spun onto the samples at 3000 rpm for 1 minute, followed by soft bake directly on the 170 ºC hotplate for 90 s. Using the EBL patterning conditions discussed in Section 4.1.6, the different feature sizes can be obtained. Similarly, the samples then were etched using the same RIE and HF conditions as the samples created by the photolithography method.

4.2 AFM and SEM Imaging of the Diode Structures

AFM and Scanning Electron Microscopy (SEM) were used to obtain the geometry and structure of the samples. The cross-section SEM images of the samples were taken at 30 keV electron beam energy using a Raith150 system [2]. AFM images from various positions on the samples, including inside the 6 μm holes and on top of Si layer were obtained using Si probe tips (non-contact Si tip with radius ≤ 10 nm, angle 10º at apex). The cross-section SEM image of a sample in Figure 4-4 shows an undercut structure of the SiO_2 layer of approximately 400 nm in depth using the HF etching process. A plan view SEM image shown in Figure 4-5 illustrates 6 μm diameter holes on a 10 μm pitch pattern formed on the top Si layer. The SEM image shows that the features have not been etched through to the underlying Si surface or at 660 nm depth because of the insufficient HF etching duration, which for this sample was 60 s. Certainly the longer HF etch duration will improve the feature profiles. In later experiments, the best possible HF etching duration was 110 s as discussed in section 4.1.5.

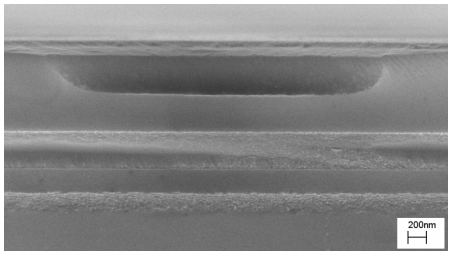


Figure 4-4 Cross-section SEM image of a 6 µm diameter hole.

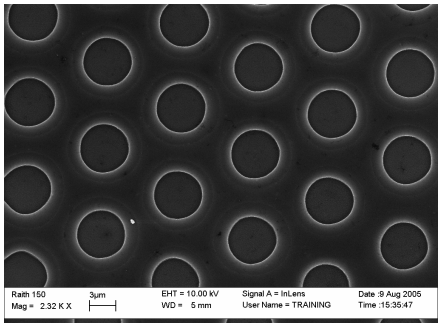


Figure 4-5 Plan view SEM image of 6µm diameter holes on a 10 µm pitch.

After the etching process, the samples were examined using AFM to measure the diode features and their physical dimension. The required depth is 660 nm since the thickness of the top Si layer and SiO_2 layer are combined to be 660 nm. However, the depth of the diode structures shown in Figure 4-6 is approximately 512 nm. It is possible that while SiO_2 was etched by wet etching process, i.e. HF etch, the top Si layer was also etched with a slower rate than the SiO_2 layer. It is also possible that the device was not etched completely as with the device in Figure 4-4, or that the AFM height measurement was not calibrated accurately at that particular time because AFM critical setting was adjusted by mistake and it was not possible to obtain the same surface profile again once nanowhiskers were grown on the sample.

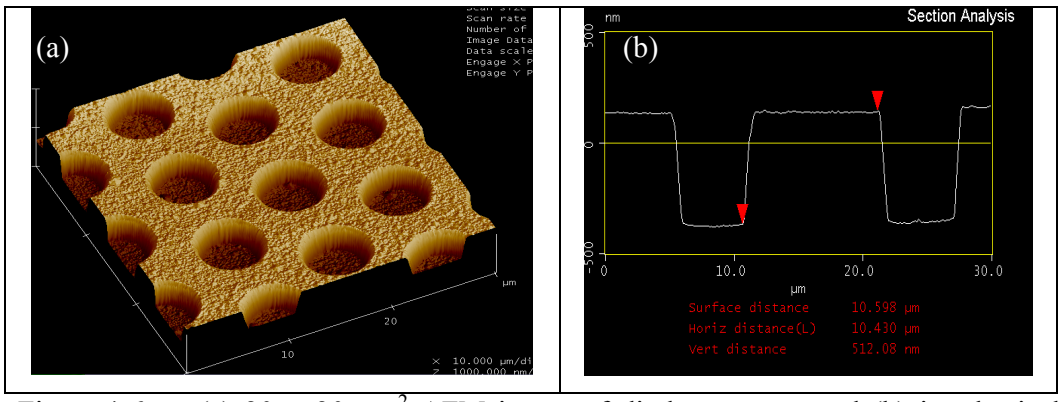


Figure 4-6 (a) 20 × 20 μm^2 AFM image of diode structure and (b) its physical dimension.

4.3 Surface Characteristics

As mentioned in Chapter 2, nanowhisker formation was initiated by the surface disorder as a result of void growth and oxide desorption. The difference between nanowhisker growth on a pristine Si surface and the growth on the underlying surface of the SOI wafer was of particular interest here, as the surface disorder is expected to be significantly different. During the annealing process, the mass transport of Si adatoms occurs on the exposed Si surface. Furthermore, the attachment and detachment of Si adatoms also affect the surface characteristics. The three factors that affect the height of nanowhiskers grown on the Si surface are annealing temperature, cooling rate and annealing duration. In order to fabricate the field emission diodes using silicon nanowhiskers as the field emitters, the diode-structured samples were sent to GNS for growing nanowhiskers using the EB-RTA decomposition technique. These samples were annealed at different annealing temperatures and duration using a raster scanned, 20keV electron beam with the heating and cooling rate of ±5ºC per second.

4.3.1 Height of Nanowhiskers and Distribution Density

The physical appearance of nanowhiskers is described by their height, shape and density. As discussed in Chapter 2, the height, shape and density depend on the annealing temperature and duration. Before and after the annealing process, the images of the sample surfaces were obtained using AFM, and example images are shown in Figure 4-7 for a sample annealed at 1100 °C for 90 s.

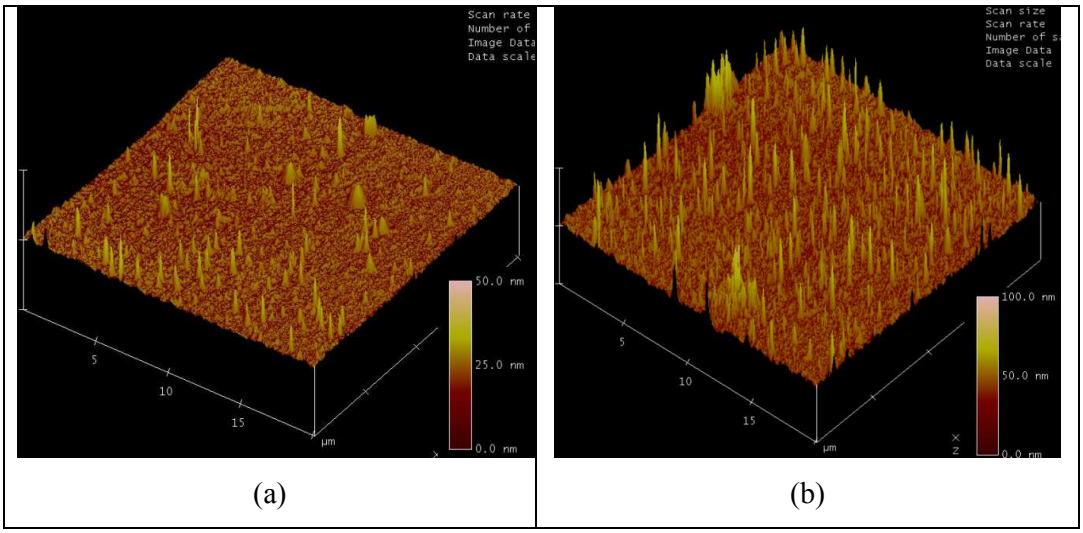
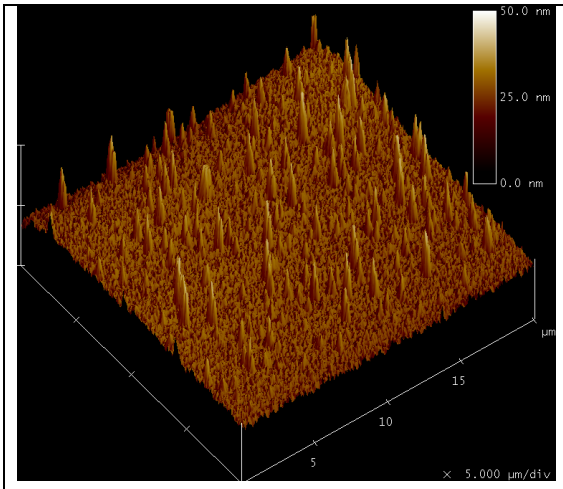


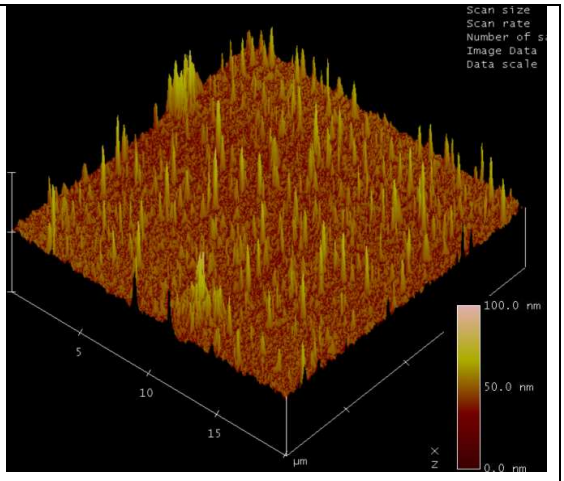
Figure 4-7 AFM images of the samples (a) before and (b) after annealing at 1100 ºC for 90s.

The surface characteristics after annealing reveal that randomly distributed nanowhiskers were grown on the Si layer. Before annealing, the surface of Si layer was rough due to the randomness of the gas ions bombarding the Si substrate during the RIE process and the inherent roughness of the Si/SiO_2 interface in the SOI wafer. After the samples were annealed for 90s, the nanowhiskers were formed due to surface disorder and they appeared to have higher density and longer dimensions than that on the control sample.

To investigate the influence of annealing temperature on the nanowhiskers' height, the experiments were performed having samples annealed at two different annealing temperatures, namely 900 °C and 1100 °C. It has been observed that the higher annealing temperature produces higher and bigger nanowhiskers but having lower density distribution as shown in Figure 4-8.



(a)



(b)

Figure 4-8 AFM images of nanowhiskers grown on the Si surface at (a) 900 °C for 45 s where maximum nanowhiskers height is 12 nm and (b) 1100 °C for 45 s where maximum height of nanowhiskers is 25 nm.

Figure 4-8 confirm the GNS claim that annealing temperature influences the nanowhiskers' height and density [56]. At lower temperature, the Si surface has shorter and smaller nanowhiskers due to the lower thermal energy which induces lower Si monomers and oxygen reactions resulting in lower number of voids and oxidation desorption. On the other hand, at higher annealing temperature the nanowhiskers are higher and larger because of higher activation energy which generates more reactions between Si adatoms and oxygen. Hypothetically, having higher number of voids grown and oxidation desorption on the Si surface, higher nanowhiskers should be observed.

By inspection, these nanowhiskers are completely isolated from each other. There is a flat and smooth area between two adjacent nanowhiskers which is referred to "flat region" as shown in Figure 4-9. These flat regions are believed to be caused by silicon adatoms migration that has been discussed in Chapter 2.

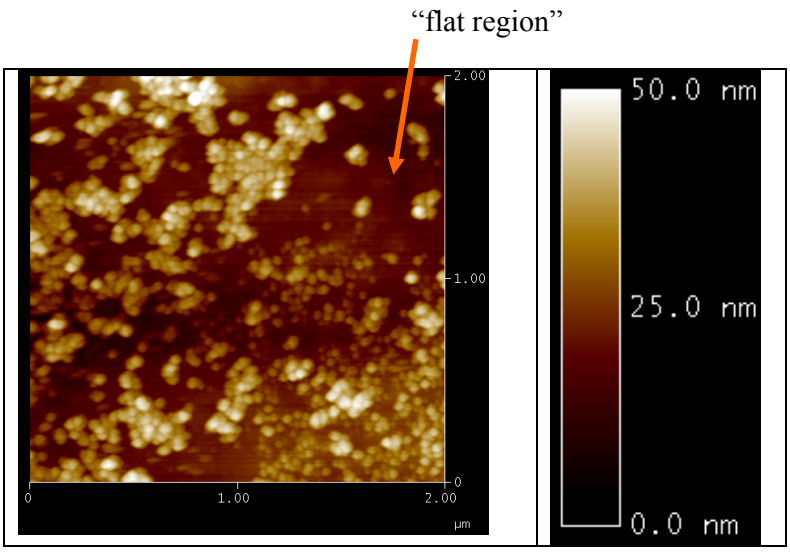


Figure 4-9 A 2µm-scan size of AFM image showing nanowhiskers among the flat regions from the sample annealed at 900 °C for 45 s.

Nanowhisker height distributions have also been determined from AFM scans [65]. The histogram of nanowhiskers heights of Si surface inside the 6µm holes on the diode structures is shown in Figure 4-10. The average of nanowhisker height is 5.6nm with the average distribution density of 30±1 μm^{-2} after the sample has been annealed at the temperature of 900 °C for 15s. Before annealing, the Si surface is not completely flat. By using particle analysis it can be seen that there are some islands on the surface possibly due to the reactive ion etching process or inherent roughness as mentioned earlier. However, it is clear that after annealing, the nanowhiskers with the height range from 3nm to 12nm were grown on Si surface.

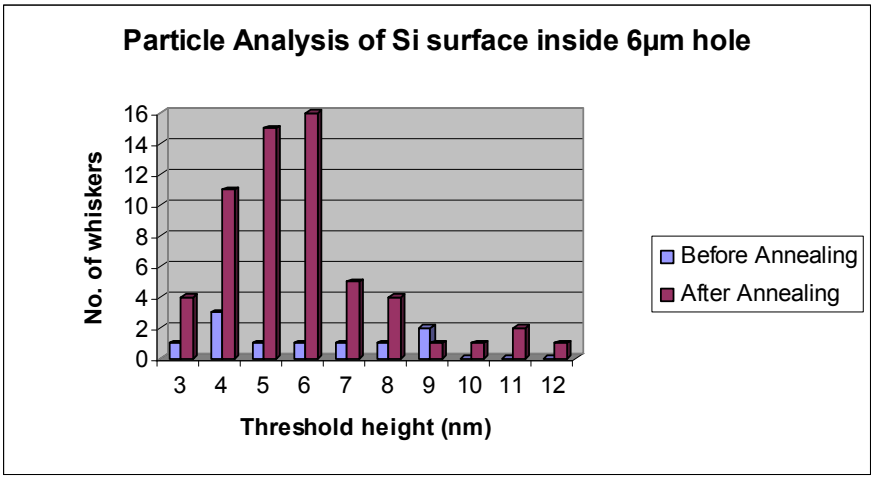


Figure 4-10 Particle analysis of 2µm scan size Si surface inside 6µm hole of the sample before and after annealing at 900°C for 15 s.

At higher annealing temperature, nanowhiskers are expected to be higher than that of which annealed at lower temperature. Figure 4-11 indicates that nanowhiskers grown on Si surface that has been annealed at the temperature of 1100 °C for 45 s have the height range from 10 nm to 25 nm with an average height of 15 nm with density of 12±1 μm^{-2}. In conclusion, higher annealing temperature can produce higher silicon nanowhiskers with a lower distribution density.

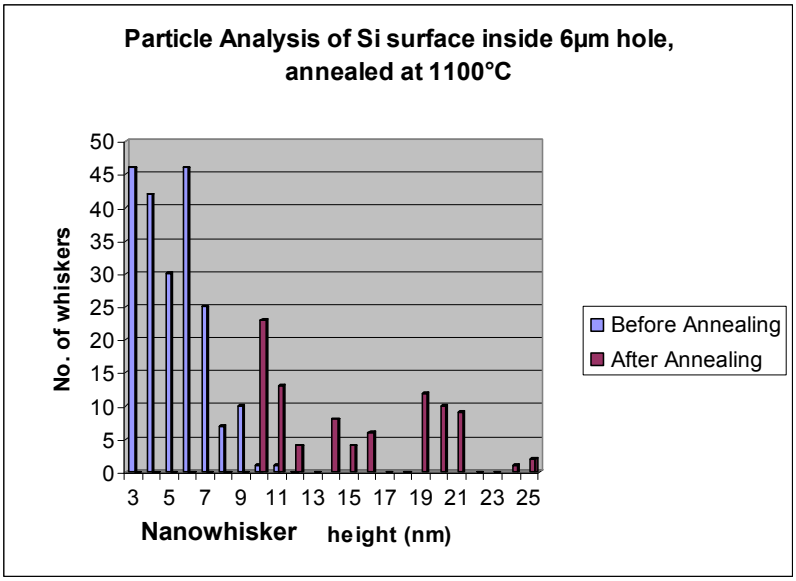


Figure 4-11 Particle analysis of 2µm scan size Si surface inside 6µm hole of the sample annealed at 1100°C for 45 s.

4.3.2 Nanowhiskers height and annealing duration

In this study, we have experimented with several different annealing durations and temperatures, namely 15 s, 45 s, and 90 s at 900 ºC or 1100 ºC. Table 4-6 summarizes the average height of nanowhiskers according to different annealing times and temperatures, where it can be seen that 35-nm long nanowhiskers are formed in a 90 s anneal at 1100 ºC, for example.

Table 4-6 Nanowhiskers average height according to different annealing times and temperatures.

Annealing Time (s)	Temperature	
	900 ºC	1100 ºC
15	5.6 nm	10 nm
45	20 nm	25 nm
90	30 nm	35 nm

From Table 4-6, the highest nanowhiskers were obtained at annealing temperature of 1100 °C for 90s. Higher nanowhiskers may be obtained using higher temperature and longer annealing time but in the semiconductor industry damage and diffusion may occur when the integrated circuit undergoes high temperature annealing for an extended period (exceeding the so-called thermal budget) [66]. Thus, the reasonable conditions for nanowhiskers growth suitable for this application would be 900 °C for 45 s resulting in 20-nm high nanowhiskers on average. Moreover, the shorter annealing time is preferred for the time efficiency. However, the results from Table 4-6 oppose the results from GNS that annealing duration has no significant effect to the height of nanowhiskers for 900 °C annealing. The average nanowhisker height of the SOI samples annealed at 900 °C increases slightly according to the annealing time.

In addition, the results from Table 4-6 also indicate that the Si nanowhiskers grown on SOI wafer are higher than those obtained on pristine Si wafer that are approximately 7.4 nm high on average [19]. This emphasizes an advantage of growing Si nanowhiskers on the SOI wafer as the higher nanowhiskers can improve the field emission.

4.4 Electrical Measurement Results

Electrical measurement of the diodes was performed using a Hewlett Packard HP4155A Semiconductor Parameter Analyzer in order to obtain Current-Voltage (IV) characteristics for field emission in an air ambient inside an electromagnetically shielded probe station. The 40-nm thick aluminium contact was first deposited at the back of each sample using thermal evaporation. By placing the devices upside down on an Al-coated glass slide, the emitted current due to applied voltages of -40V to 40V was measured from the cathode to the anode as shown in Figure 4-12. These measurements provided control data prior to nanowhisker formation. After the samples had been annealed, their electrical characteristics were investigated again. Results are presented in terms of current versus macroscopic field E ($V\mu m^{-1}$), which is calculated by dividing the applied voltage by the distance between the Al anode and the Si cathode.

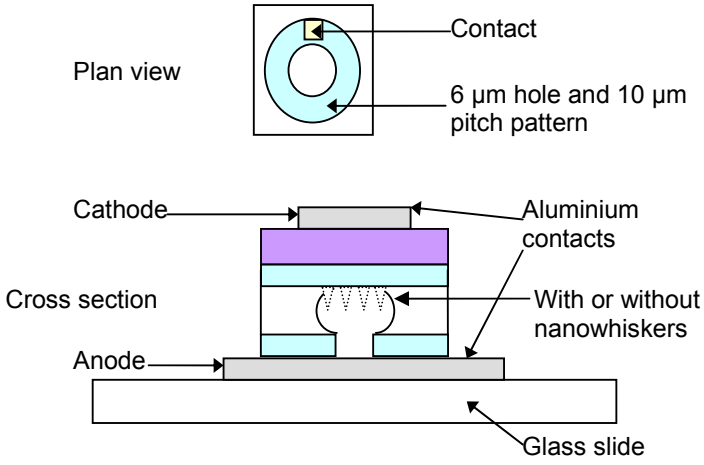


Figure 4-12 Schematic diagram of electrical characteristics measurement.

A typical current versus macroscopic electric field result for a control sample is shown in Figure 4-13. There appears to be a small current offset of the measurement apparatus, however it can be seen that the applied electric field is inadequate for field emission to occur from a non-nanowhisker based cathode, with currents below 1nA in all cases.

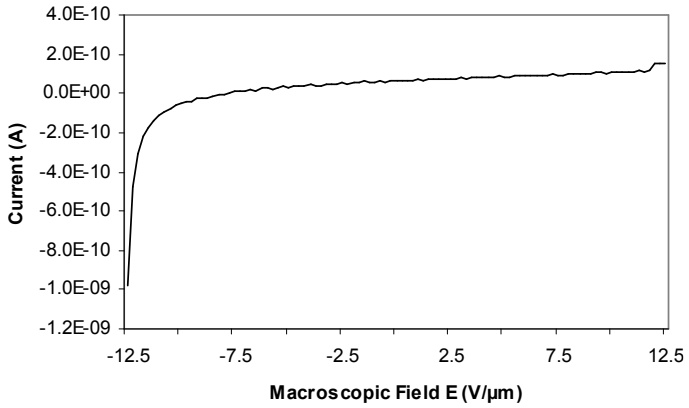


Figure 4-13 Conduction characteristics of a diode structure without nanowhiskers.

To obtain the field emission characteristics, emission currents were measured from the positive biased anode by applying dc voltage to the base electrode (anode) relatively to grounded cathode electrode in order to extract electrons from the nanowhiskers. The field emission measurement results for 4 consecutive sweeps of the anode voltage are displayed in Figure 4-14 for a device annealed for 15 s at 1100ºC (5.6-nm high whiskers on average). All curves show rectifying behaviour typical of a field emission diode. A sharply-rising current was observed when the nanostructures are present on the cathode surface indicating that field emission from nanowhiskers exceeds the background current of 1nA (in this case the leakage current through the insulator layer), and currents up to 1µA were recorded.

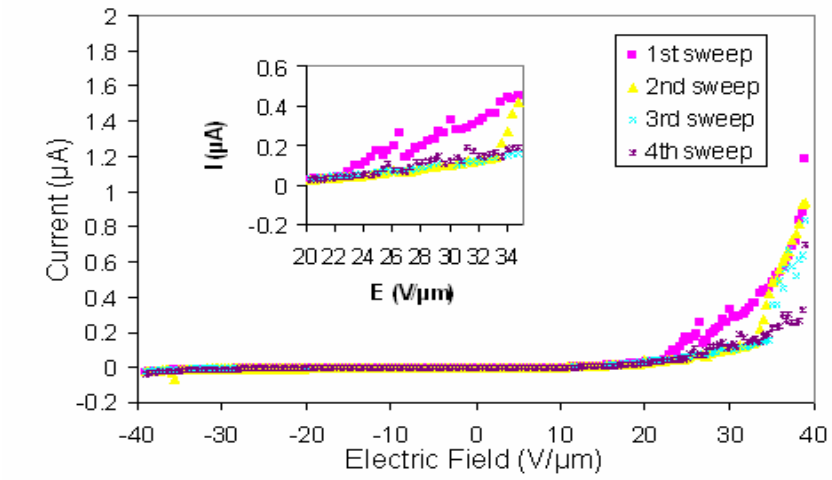
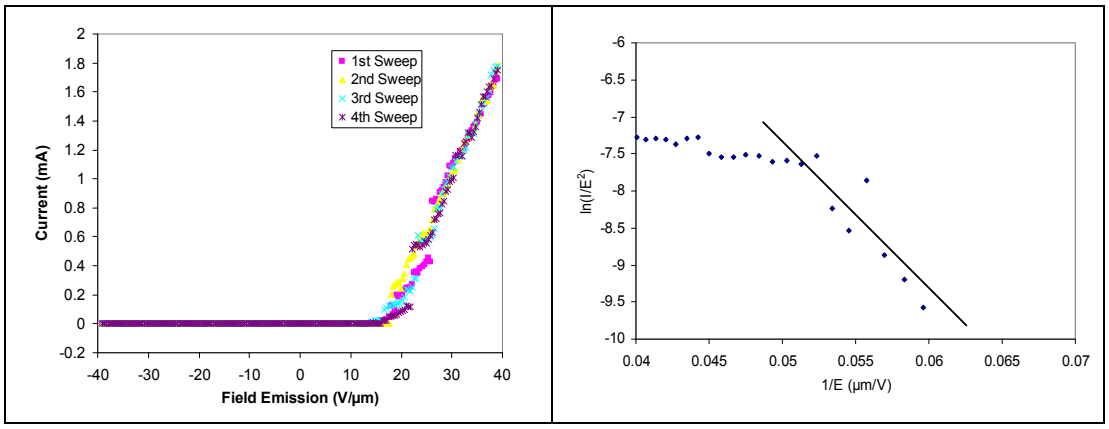


Figure 4-14 *I-E* characteristics of silicon nanowhisker field emission diode which was annealed for 15 s at 1100 ºC. Inset: expansion of turn-on region.

The turn-on electric field at which electron field emission occurs was found to increase from 22 V/µm to 28 V/µm between the first and the last cycles respectively as shown in the inset of Figure 4-14. Figure 4-14 shows that the maximum emitted current for 40 V/µm is approximately 0.9µA according to the short nanowhiskers of approximately 30nm grown on Si surface. The maximum emitted currents of a field emission diode annealed for 90s at 1100 ºC were approximately 1.8mA as shown in Figure 4-15(a). Thus the longer annealing time and temperature promote higher field emission currents since there are longer nanowhiskers grown on cathode base. Figure 4-15(b) indicates that the conduction though Fowler-Nordheim tunnelling process occurred by having approximately linear relationship of $1/E$ versus $\ln(I/E^2)$ at fields up to 20 V/µm.



(a) (b)

Figure 4-15 (a) I-E characteristics of silicon nanowhisker field emission diode which was annealed for 90 s at 1100 ºC, (b) Fowler Nordheim plot [$\ln(I/E^2)$ versus 1/E] of nanostructured diode.

This study was done under atmosphere environment whilst typical field emission devices must be operated under vacuum conditions in order to suppress scattering of the emitted electrons and sputtering of the cathode by ionising electron-molecule collisions [67]. The short anode-cathode distance will result in few scattering events. However the vacuum operation of this device can be studied in the future.

4.5 Samples with EBL Pattern

To gain more understanding about the electrical characteristics of field emission diodes and improve the electrical contact pad system, a better device layout was designed using a four-area isolation mask as shown in Figure 4-16. The first isolation contains only a Nichrome contact pad on the Si surface. The second isolation has EBL patterns written on using an electron beam with a current of approximately 177pA and dose of 216 $\mu A/cm^2$. Three different pattern sizes, namely 2µm feature on 10µm period, 5µm feature on 25µm period and 10µm feature on 50µm period, were used to investigate the effect of the feature size on the emitted current.

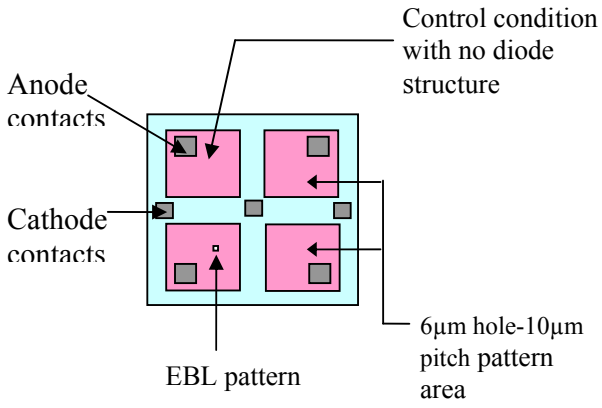


Figure 4-16 Four-isolation devices

The three square patterns of the EBL-formed diodes shown in Figure 4-17 were obtained by atomic force microscopy after the devices were annealed for 45 s at 1100°C. It can be seen that the top surface of each image on the left has similar roughness. On the other hand, the surface inside each square feature appears to have no significant nanowhiskers. Moreover, the islands that have been grown are not sharp and dense as expected. This may be caused by the defects in the etching process. These EBL patterns were created by using PMMA as a mask which may not be thick enough to withstand the RIE etching process resulting in surface deep penetration. As shown in Figure 4-17, there are small holes in the top surface as well as the surface inside the square pattern. The bigger square features, i.e. 10µm holes, tend to have rougher surface than the smaller one. However, no significant nanowhiskers can be seen in any of the three patterns.

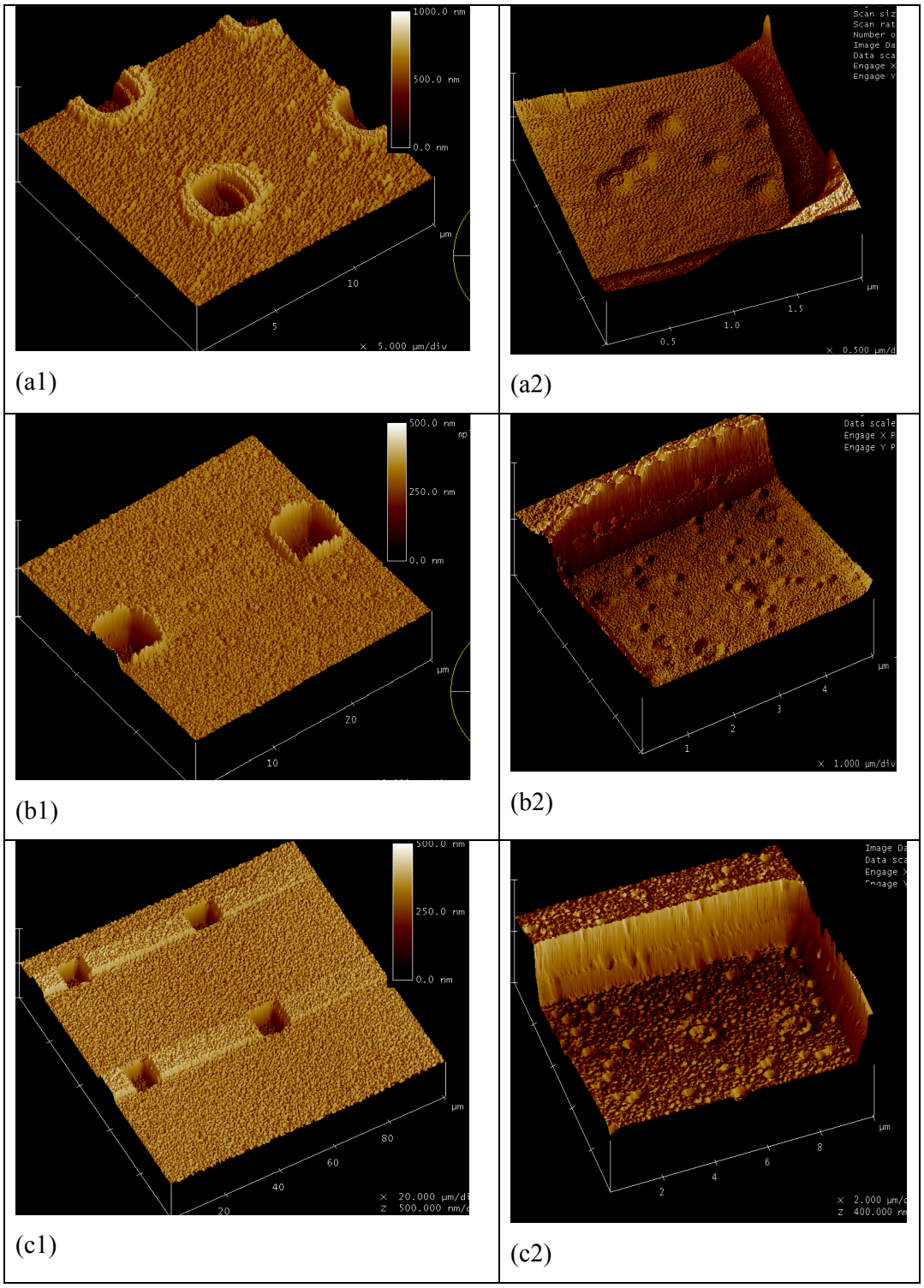


Figure 4-17 Electron Beam Lithography patterns, (a) 2μm feature on 10μm period, (b) 5μm feature on 25μm period, and (c) 10μm feature on 50μm period.

On the right hand side of each pattern is its AFM image of the surface inside the square feature. The electrical measurement for this set of samples was done similarly to the previous method except dc voltage can be applied directly to the cathode and anode contacts on the sample without using the glass slide. Unsurprisingly, the electrical characteristics of these set of samples are not diode-like as illustrated in Figure 4-18. This confirms that the field emission did not occur as expected due to the absence of nanowhiskers or emitters. The electrical characteristics were obtained by applying voltages from -40 V to 40 V. The measured maximum current shown in this figure is 900 pA which is a very small value, similar to the control samples.

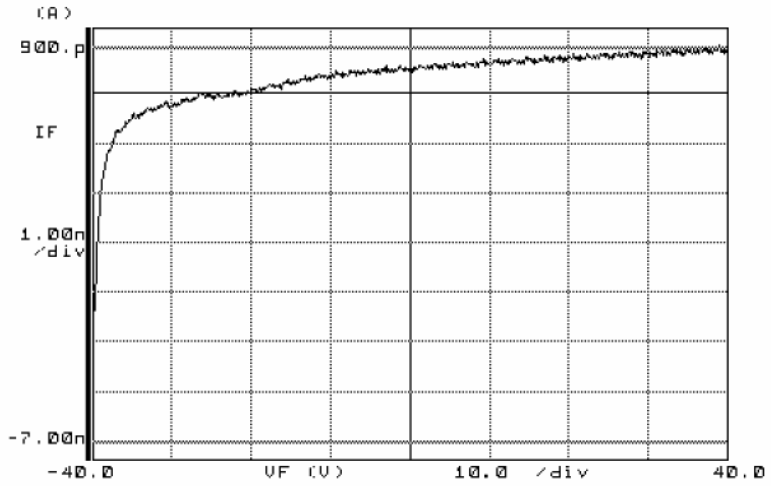


Figure 4-18 Field emitted current of a sample having 2µm features on 10µm period which was annealed at 1100 °C for 45s.

4.6 Leakage Current

Leakage current in the electrical measurement system was observed on some occasions where the surface of the samples have no nanowhiskers, for example one of the samples that were annealed at 900 °C for 15 s. To test the leakage current in this system, a negative bias voltage (0V to -20V) and positive bias voltage (0V to 20V) was applied and then recorded as shown in Figure 4-19. The current of -100nA with the bias voltage of -20V was observed while the current of 120nA was obtained when bias voltage of 20V was applied. However, this leakage current is not significant as it is only in nanoscale compared to the maximum emitted current that is up to 1.8 mA, i.e. millions times smaller, so it can be neglected.

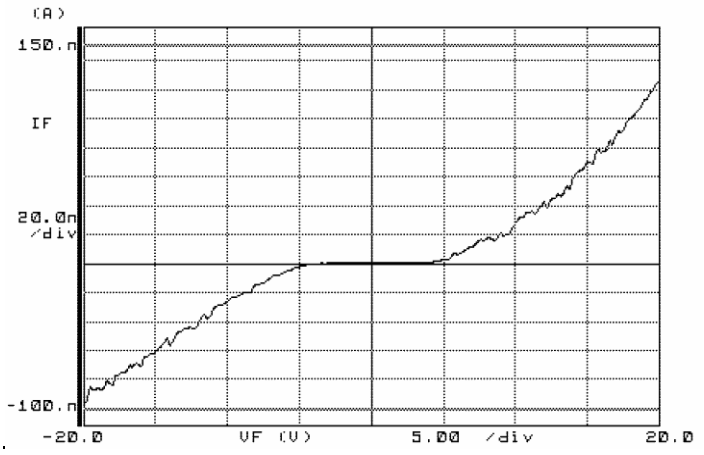


Figure 4.19 Electrical measurement set up leakage current test

Leakage current is also observed for field emission diodes in some cases where the diode structure has straight sidewalls or sidewall contamination causing some kind of diode-like connection between anode and cathode, such as the samples which the SiO_2 layer has not been etched with HF etching process for 30 s after RIE. The applied voltage ranged from -40 V to 0 V has some reverse leakage current up to -0.4 mA as shown in Figure 4-20. This may occur because the silicon dioxide becomes charged during the measurements. Moreover, degradation of the emitters is observed and will be discussed in the next section.

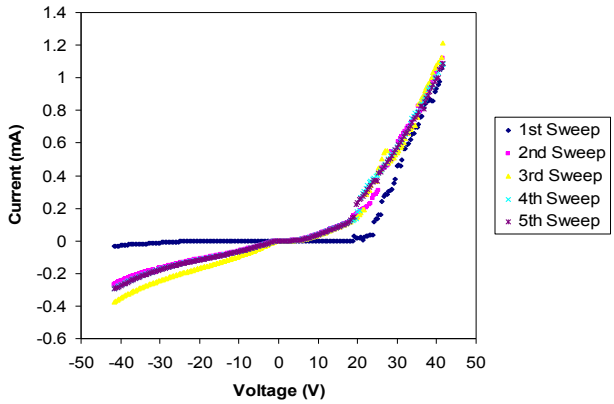


Figure 4-20 I-V characteristics of a sample annealed for 45 s at 900 °C with applied voltage from -40V to 40V.

4.7 Lifetime and Stability Test Results

One of the primary reasons that field emission devices have failed to emerge as a new alternative field emission displays in the market has been their reputation for poor reliability. Therefore lifetime and stability of the two best diodes produced in this study have been tested by applying a constant voltage for a certain period of time. Figure 4-21 shows the current stability at constant applied voltages of 0.8V and 2V for 100s. At lower applied voltage, the emitted current is not only lower, but also has lower frequency noise. Over a short period of time, the emitted current due to voltage lower than 2V appears to be stable as shown in the figures below.

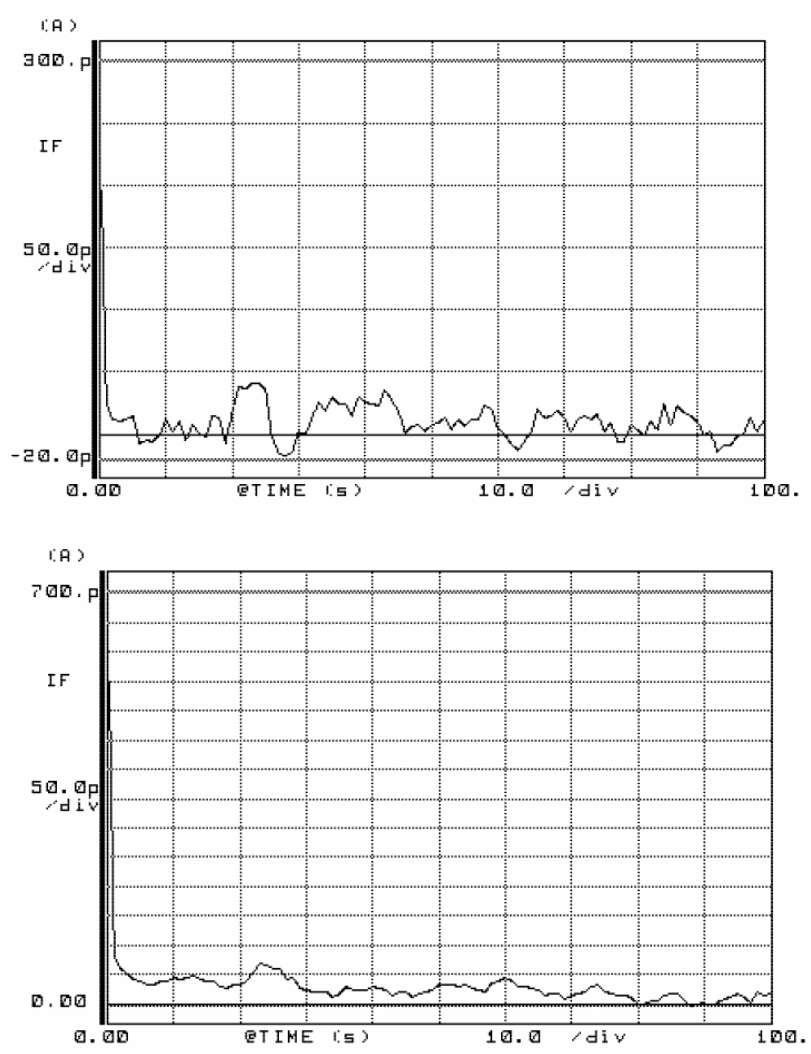


Figure 4-21 Current stability versus time for the diode at applied voltage of (a) 0.8V and (b) 2V for 100s.

However, the emitted current appears to be unstable at higher applied voltage. Figure 4-22 shows a current stability of a diode that has been tested at 20V for 1 hour. It indicates that at higher emitted current, stability of the diode degrades over time. For this particular device, the emitted current drops down to approximately 1.5 μA at the 40th minute. At high applied voltage, a catastrophic breakdown event may occur and take place at the site of emission, often damaging the emitters on the cathode leaving melted nanowhiskers as a result of higher current emitted at the tips for a long period of time. The presence of oxygen when the measurements were performed in atmosphere is likely to be one of the reasons that cause the emitters to be oxidised during prolonged operation resulting in degradation.

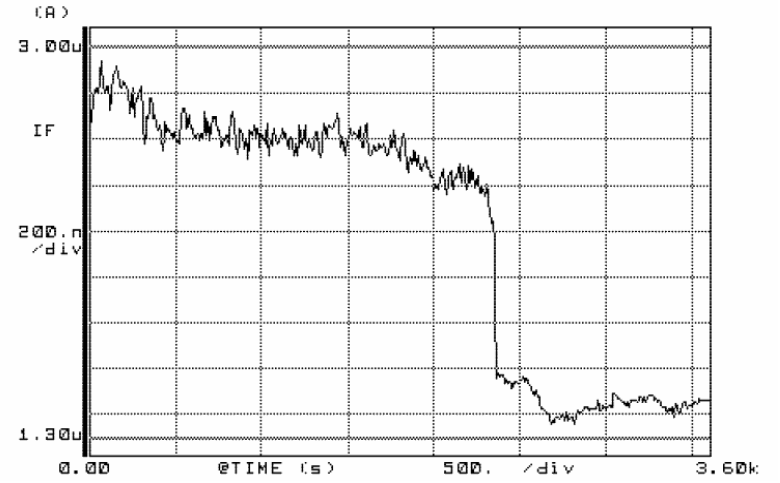
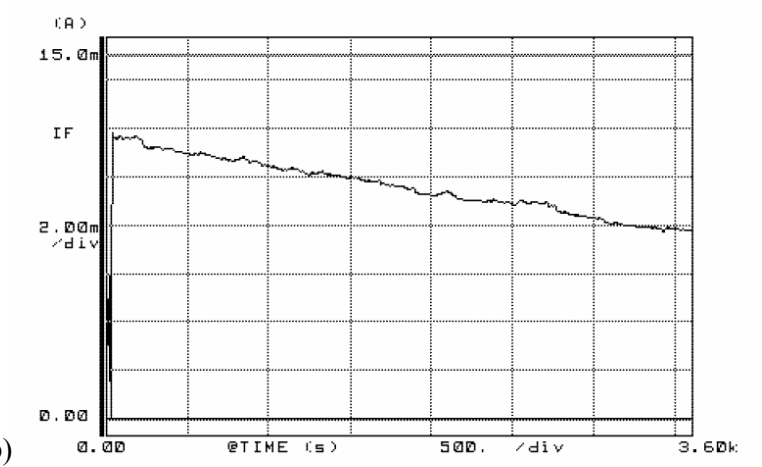


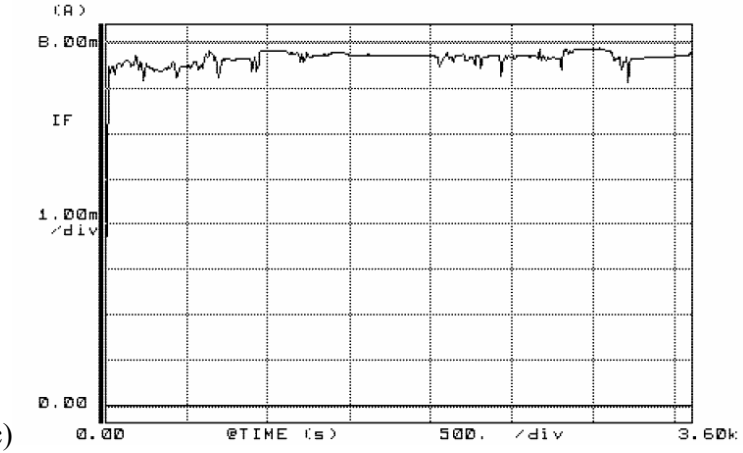
Figure 4-22 Current stability versus time at 20V for 1 hour.

Another result observed in this study is the current stability at a constant applied voltage depended again on the current (Fig. 4-23). Figure 4-23(c) shows that at low emitted current (< 7.5μA) and low voltage applied, the current switched between discrete current level with the period as long as 1000s. The frequency noise appears to increase with the current. At emitted current of 12mA as shown in Figure 4-23(a) has high switching frequency and the emission becomes gradually stable, without detectable discrete level, while at 8mA (Fig. 4-23(b)) the current has switching period of approximately 500s. The degradation of emitters is one of the issues that has to be considered and improved for this study. More investigation can be done for longer measurements such as 1000 hours, but with limited equipment availability, this was difficult to achieve.

(a)



(b)



(c)

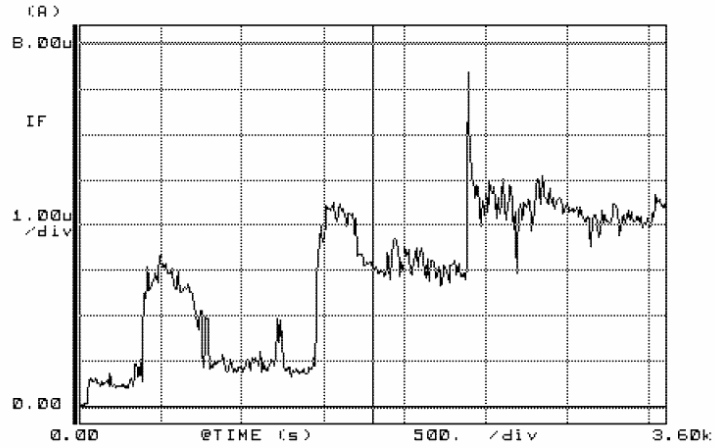


Figure 4-23 Current stability versus time for the best device at applied voltage of (a) 40V with maximum emitted current of 12mA, (b) 20V with maximum emitted current of 8mA and (c) 1V with maximum emitted current of 7.5μA.

4.8 Light Emission on Phosphor Screen

Many research groups have reported that phosphor screens, which are very easy to produce and inexpensive, are suitable for testing the light emission induced by field emission devices [68-72]. Field emission represents a type of quantum tunnelling in which electrons pass through the barrier in the presence of high electric field. Unlike thermionic emission, field emission does not require high temperature for extracting electrons. The field emitted current strongly depends on the emitter material and its geometry. One of many applications of field emission diodes is field emission displays. Hence to investigate whether this diode based on silicon nanowhiskers is an excellent alternative, a simple field emission on phosphor screen test was performed. Phosphors are solid luminescent materials that emit photons when exited by an external energy source, such as Electron beam or UV light [73,74]. Phosphors are composed of an inert host lattice, which is transparent to the excitation radiation, such as oxides, sulfides, selenides, silicate of zinc, cadmium, manganese, aluminium, silicon or other rare earth metals, and an activator, which is excited under energy bombardment [75]. The process of luminescence occurs by the absorption of energy at the activation site, relaxation, emission of a photon and a return to the ground state.

Keke Huang, a third professional year student in our department, tested the devices produced in this research by using a provided phosphor screen. The schematic diagram of the experimental set up consists of three main parts: diode, phosphor screen and voltage supply as shown in Figure 4-24.

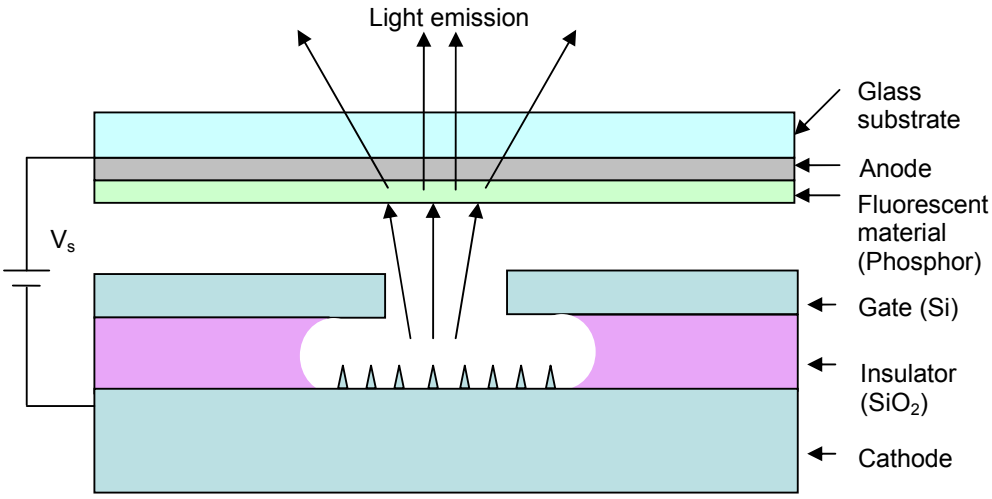


Figure 4-24 Schematic of field emission display

The tested samples have emitted current of approximately 1.8 mA/cm^2. This value is strong enough to create light emission, however no observation of light emission has been reported by the student. The reason to this unexpected result is perhaps the bad electrical connections which surely can be improved in the future.

4.9 Summary

The objectives of this research are to develop the fabrication process for field emission diodes based on silicon nanowhiskers, investigate their electrical characteristics, stability and light emission characteristics. By using the process described in Section 4.1, a number of diodes were fabricated and investigated by using AFM. The fabrication process for this diode structure is efficient and good enough to produce at least 80% success rate. Before sending the diode devices to GNS for nanowhiskers growth, some electrical measurements and AFM images were obtained. After growth the samples have evidently shown the expected results regarding nanowhiskers height, distribution density and physical appearance. This is encouraging as nanowhisker growth on SOI material had not been reported previously. The nanowhiskers on the samples which have been annealed at higher annealing temperature were higher and denser. However, the annealing duration shows a slight effect on the nanowhiskers height.

Electrical characteristics of the devices indicate that they have diode-like behaviour with low leakage current at the negative bias and high emitted current up to 1.8mA where positive voltage was applied. The degradation of the devices has been observed as after several sweeps the emitted current was reduced and the turn-on voltage was increased. However, the degradation was not significant as there is only slightly difference between each sweep.

Stability and life time were also determined by applying a constant voltage for a certain period of time. The constant applied voltages ranged from 0.8 V to 40 V. It turned out that at lower applied voltage, the emitted current was lower. Though at lower emitted current, it fluctuated with discrete-like levels of switching, with a long period of up to 1000 s. At higher emitted current, it appears to be more stable with a high switching frequency. Over an hour of measurement, the emission current

appears to be stable. There were promising results from these samples but the light emission on phosphor screen was not achieved. This is an issue which requires further investigation.

CHAPTER FIVE

DISCUSSIONS

In the previous chapters, the fabrication techniques, experimental results including Si surface analysis, electrical characteristics and stability have been discussed. Some experimental issues emerged due to some practical limitations of the experiments and these will be discussed in this chapter. Further, some possible applications will also be covered to give the ideas of what nanowhiskers can be applied to in the future. Finally, some suggestions for the future work that may improve the devices are also presented.

5.1 Experimental Issues

It is very important to address any experimental issues or problems that were encountered throughout the research with the purpose of providing some useful information for further research. A few problems were experienced during diode structure fabrications, such as material properties, photolithography and etching issues, electrical measurement equipment sensitivity and AFM issues. These problems may be avoided or improved as suggested in the next section.

5.1.1 Material Properties

During the photolithography part of the fabrication process, suitable photoresist was the main issue that needed to be considered. The photoresist used in this research was AZ 4620 (Clariant Corp.) which is rather thick, so the appropriate spinning speed was crucial. When the photoresist has been left in the small bottle for a period of time, it tends to be thicker. As a result, the spinning speed was required to be reduced to get samples completely covered. The alternative is to add some resist thinner, but this may cause further issue regarding the unknown thickness of the resist.

In addition, a thick 8% PMMA was used as a mask in the reactive ion etching process for the second set some samples with direct EBL patterning. This PMMA was quite thick when it comes to writing EBL patterns; this resulted in charging effects which make it difficult to find the focusing spot, i.e. dust particle, for focusing and eliminating stigmatism. In addition the thick resist made it difficult to obtain a good electrical connection of the sample in the EBL system. When the samples were put into the chamber, a bit of a movement of the clip to scratch the thick PMMA at the particular area for better contact should be applied to reduce charging effects during the pattern writing. More issues on EBL will be discussed later.

5.1.2 Photolithography and etching Issues

During the mask alignment process, there were some problems to determine the precise location on the sample surface where the mask was applied. Care should be taken to make sure that the mask area is in the middle of the sample. Long exposure of UV light was applied to expose through the thick layer of photoresist. An issue regarding reactive ion etching was that the long etching time causes the table temperature to rise; on some occasions liquid nitrogen was used to bring the temperature down to room temperature (295 K). Moreover during the HF etching process, all the plastic containers and tweezers must be used at all times. HF is hazardous chemical that can cause a severe effect to bone tissue, so this process should be performed only when there was someone around in case of emergency.

5.1.3 Electrical Measurement Equipment Sensitivity

It appears that the electrical measurement results strongly depend on the probe contacts. Some dramatic changes were observed while recording an electrical measurement, when there was noise or some vibration occurred close to the probe station area. This can be reduced by taking measurements in a closed compound. Thicker contact pads can also be applied to promote a better contact because after taking measurements for a few times, contact at particular point was worn off.

5.1.4 Atomic Force Microscopy Issues

The sharpness of AFM tips has critical effect on the quality of their scan images. Although in tapping mode the tips are not worn easily, AFM tips should be changed from time to time, i.e. 4-5 hours of intense scanning. The resolution of the images depends strongly on how the tip was set up and also the laser focusing step. It was quite difficult to focus the laser to the exact position of the tip at the beginning; however, this issue was reduced when more experience was gained.

5.2 Application of Nanowhiskers

As discussed in Chapter 1, the vacuum microelectronics require cold cathode emitters and nanowhiskers properties have enormous potential to compete with the present materials such as carbon nanotubes. Carbon nanotubes have attractive field emission properties due to their elongated and thin shape, but their cost and difficulty in handling and fabrication process are some disadvantages that limit their ability to be used widely in the commercial sector [76]. Nanowhiskers are on the other hand a lot cheaper to produce, and along with their uncomplicated fabrication, offer them enormous opportunity in the future for many application including field emission display, light sources, and high power and frequency devices [1-4].

5.2.1 Field Emission Display (FED)

Flat panel display is a very booming industry at the present. After a long era of the bulky Cathode Ray Tube (CRT), which has been around since 1897 [76], some new technologies have emerged including FED, Liquid Crystal Display (LCD), Plasma Display Panel (PDP), Organic Light Emitter Display (OLED), Surface Conduction Display (SED) [77] and Nano-emissive Display (NEDs) [78,79]. Many of these possible contenders are not well developed including FED.

Compared to the alternatives, silicon nanowhiskers produced by GNS fabrication techniques are simple, fast to grow and low cost as discussed in Chapter 3. A highly uniformity distribution of the silicon nanowhiskers is observed on both normal Si (100) and SIMOX-SOI wafer. In Chapter 4, some characteristics of the diode

structure devices were discussed which include its high field emitted current up to 1.8mA/cm^2 and low turn-on voltage of less than 10 V. These make silicon the nanowhiskers a promising candidate for FEDs.

As mentioned in Chapter 4, silicon nanowhiskers have degraded after high voltages applied for a period of time can be one of the drawbacks, and this requires further investigation and improvements in the future. Since this research has only studied the electrical characteristics of silicon nanowhiskers in atmosphere, the vacuum environment must be applied for further investigation to search for better performance.

5.2.2 Light Sources

A field-emission light source produces light by bombarding phosphor layer with energetic electrons emitted by a cold cathode. Light sources with field emitters promise an interesting alternative to fluorescent lamps. Bonnard and Croci realised fully sealed elements can replace their fluorescent counterparts [80]. In comparison with fluorescent tubes, nanotube-based field emitting light sources are mercury free, start up with instantly and are dimmable. They give higher brightness than normal fluorescent elements. Hence nanowhiskers can be an alternative of nanotubes in this case.

ISE Electronics Corp. uses carbon nanotubes as field emitters in outdoor advertising panels, giving higher brightness but lower power consumption, and longer time expectancy than normal fluorescent elements [80]. Nanowhiskers have very similar properties; hence they could be applied in this application. Unfortunately, the light emission was not achieved with this silicon nanowhiskers based devices as discussed in Chapter 4. The main reason for these results is the degradation of the nanowhisker tips due to an intensive use during the electrical characteristics and stability tests. Consequently, the emitted current might be reduced down to μA/cm^2 range, which is not sufficient to be seen on this particular phosphor screen. Moreover, the electrical connections of the light emission measurements may have some faults, especially at the contact pads. In addition, the imaging method while performing that experiment may not be efficient enough to capture the light emission.

5.2.3 High Power and High Frequency Devices

Vacuum microelectronics involves controlling propagation of electrons in vacuum, aiming to obtain a specific gain of an initial electrical signal. One of the most common vacuum electronics devices is the diode. A classic vacuum tube which is based on thermionic emission is not suitable for miniaturisation and usually requires bulky vacuum packaging. Hence the alternative nanostructure-based devices are promising candidates, due to their high current densities and their response to high electrical excitation. CNT have currently been used as the cold cathode emitter. A research group has shown that vacuum microelectronics devices can operate within the frequency range of 100 GHz to 500 GHz while the solid-state devices have the maximum cut-off frequency of 100 GHz [81]. Vacuum microelectronics devices also have much higher electron energy, up to thousand times, than solid-state devices which have electron energy less than 0.3 V [81]. The sufficient vacuum condition where all or most of the gas has been removed is required to permit electrons to move with low interaction of any remaining gas molecules and decelerate the erosion of the cathode surface which is one of the factor limiting the life time of the devices. Therefore vacuum electronics devices are suitable for high power and high frequency devices. Silicon nanowhiskers may be one of the alternatives for this application, even though their time and frequency response have not been investigated here.

5.3 Improvements for Future Experiment

Throughout this research, the diode structure devices have only been tested under atmosphere environment. Some promising results in terms of high field emitted current and low turn-on voltage have been observed. Hence carrying the experiment under vacuum will improve a great deal of the field emitted current because electrons travel faster in vacuum than in atmosphere environment. A vacuum environment does not only increase the operating frequency and power efficiency; it also prevents unwanted contamination and chemical reactions that might damage the tip of emitters. The oxide growth is another problem with atmosphere environment. In air, oxygen can react with Si forming silicon dioxide that can reduce field emitted current. For better understanding of nanowhiskers characteristics, a vacuum system should be

employed in the electrical measurements. From Chapter 4, it can be seen that silicon nanowhiskers provide high emitted current up to the mA level, reasonably stable over period of time in the atmospheric environment. Thus vacuum system should increase field emission, power and frequency resulting in possible expanding of its applications.

5.4 Summary

A simple diode structure fabrication process using SIMOX-SOI wafer has been developed. Even though the fabrication was straight forward and simple, there are some issues including material properties, photolithography and etching issues, electrical measurement system sensitivity and AFM tips issues that needed to be considered. With suggestions mentioned previously in this chapter, the future fabrication problems can be prevented.

The field emission and stability properties, simplicity of fabrication and cost efficiency of silicon nanowhiskers have attracted attention from many research groups. Several possible applications of silicon nanowhiskers are FED, light sources and high frequency and power devices have been discussed. Even though nanowhiskers does not provide higher field emission than CNTs, their other advantages mentioned previously and their compatibility to the existing CMOS technology can be attractive for some applications. Moreover, electrical properties of nanowhiskers have not been investigated in vacuum in this study; the chance that nanowhiskers can be improved in field emission aspect is high.

CHAPTER SIX

CONCLUSIONS

Vacuum microelectronic devices have been intensively investigated in the past decades. The previous studies focused more on field emission devices due to their unique properties of emitting electrons at low temperature with lower power consumption, which is far better than thermionic emission in some applications. In this study, GNS nanowhiskers were used as emitters in field emission diodes. To further study and investigate the electrical characteristics of silicon nanowhiskers produced by electron beam annealing, a SIMOX-SOI wafer was used to create diode structures. Then GNS nanowhiskers were grown on these devices under different conditions. Surface analysis and electrical measurements of these samples were conducted to investigate the ability of silicon nanowhiskers as alternative emitters in field emission devices. The remainder of this chapter includes the conclusion of the main experimental results and possible future directions to improve the results.

6.1 Experiments

The fabrication procedure of SIMOX field emission diodes has been developed using the simple techniques involving photolithography which transfers the diode patterns onto the samples in the specific areas, and etching the Si layer using RIE and SiO_2 layer using HF etch. These processes were developed through a number of experiments searching for suitable procedures and conditions, such as the photoresist thickness, spinning speed, UV exposure time, developing time, RIE etching time and HF etching time. After the experiments, the procedures and conditions that create optimum results for fabricating diode structures were obtained.

The results regarding surface characteristics, electrical characteristics and stability of the field emission diodes were presented in Chapter 4. In conclusion, the SIMOX-SOI samples have shown the maximum average height of nanowhiskers of 35 nm with a random density distribution of approximately 30±1 μm^{-2}. These surface characteristics are close to those obtained when a Si (100) wafer was used by GNS. This research achieved the field emission of 1.8 mA with the turn-on voltage at 20 V from our best sample. The study also illustrated that these field emission diodes are stable when the high voltage (20 V) is applied. At lower current emission, discrete fluctuations with the period of 1000 s have been observed. In contrast, at high current emission, they appear to be more stable. Stability tests were performed for up to 1 hour. However, the results from this research bring out the work that can improve and further the investigation in the future, as described below.

6.2 Future Work

The work done in this research to date focused on the field emission diode structures fabricated using photolithography with specific feature size of 6 μm diameter holes. In this case, the field emission diode features were fixed at 6 μm diameter. Although the results turned out to be reasonably good, the effect of feature size on the electrical characteristics will be an interesting work in the future. We have started this study using EBL to write different feature sizes directly onto the sample surface, but the results have failed to show a diode-like characteristics. Perhaps the contact pads for the electrical measurement should be improved. Hence, the example of possible feature sizes created by EBL is illustrated in Figure 6-1.

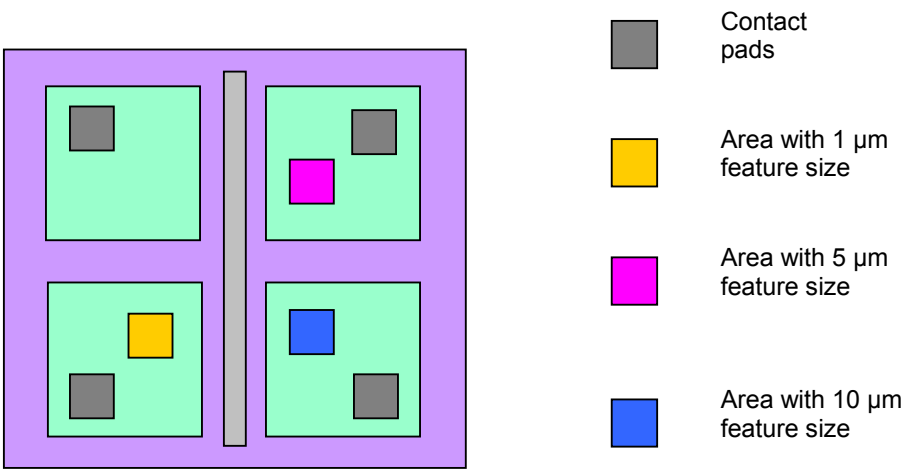


Figure 6-1 A possible arrangements for diode structure testing the effect of feature size on the electrical characteristics.

Some improvements in EBL patterning and etching process are required to produce the well structured diodes. As shown above, the top left isolation in Figure 6-1 has no diode structures for a control condition. The possible feature sizes may range from 1 µm to 10 µm. However, the smaller features are preferred as the field emission devices are moving to the smaller feature size direction. Other issues such as a vacuum chamber for electrical measurements and light emission on phosphor screen can also be considered. Further research in this area is still required to exploit the silicon nanowhisker properties and their simple and inexpensive fabrication process, aiming to improve the results and explore applications.

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APPENDIX A

Limited Source Diffusion Calculation

A total number of atoms per unit area of wafer is "dose" (S), in limited source diffusion, S is fixed. For this case the solution to Fick's equation is

$$C(x,t) = \frac{S}{\sqrt{\pi Dt}} \exp - \left[\frac{x}{2\sqrt{Dt}} \right]^2 . \qquad (1)$$

The dose is the integral of impurity concentration throughout the wafer giving,

$$S = 2C_0 \sqrt{\frac{Dt}{\pi}} .$$

The drive-in process was performed entirely at 1000 °C, the time required can be determined.

A table lists the pre-exponentials and activate energies for phosphorus diffusion:
$D_0 = 10.5\ cm^2/s$, $E_A = 3.69$ eV. Hence the diffusion coefficient for pre-deposition is

$$D = D_0 \exp\left[\frac{-E_A}{kT} \right] = \left(10.5 \frac{cm^2}{s} \right) \exp\left[\frac{3.69eV}{8.617 \times 10^{-5} \frac{eV}{K} (1273K)} \right] = 3.5 \times 10^{-14} \frac{cm^2}{s} .$$

The distance x is 280 nm to dope the phosphorus atoms onto top Si layer.
$C_0 = 5 \times 10^{20}\ cm^{-3}$, so S can be determined:

$$S = 2N_0 \sqrt{\frac{Dt}{\pi}} = 2\left(5 \times 10^{20} cm^{-3}\right) \left[\sqrt{\frac{3.5 \times 10^{-14} t}{\pi}} \right] \qquad (2)$$

t can be determined by using equation (1) and (2), resulting:

$$t = 2325 \text{ s} \approx 39 \text{ minutes}$$

APPENDIX B

Conference paper

- S Thongpang, R J Blaikie, S P Lansley, S Johnson and A Markwitz, "Field Emission Diode Based On Self-assembled Silicon Nanowhiskers Using SIMOX-SOI Substrates", *ENZCon05 at Department of Electrical & Computer Engineering, Manukau Institute of Technology, New Zealand*, *November 2005*.

APPENDIX C

Poster for Macdiarmid Institute Student Symposium in November 2005